An ASIC Implementation: Wave-Pipelined Circuit for Dual-Tree Complex Wavelet Transformation

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Abstract. In digital systems, the wave-pipelining concepts are used to achieve maximal rate of operation. A high operating frequency are obtained by adjusting the two factors called clock skew, & clock period in order to latch the combinational logic circuit output as stable. In literature, only trial & error, manual procedures are used for the choice of the optimum clock period and clock skew values between input/outputs register of wave-pipelined circuit. The major contribution of this paper is to propose automated ASIC implementation using wave-pipelined circuits to verify the proposal a dual-tree complex wavelet transformation algorithm is taken into consideration in which scheme is again carried out into 3 types i.e., Pipelining, wave-pipelining, non-pipelining. With the implementation result survey, it is observed that wave-pipelined circuits are 30% more faster than that of non-pipelining circuits, pipelined circuits are 49% more faster than that of wave-pipelined circuits but occupies 30% more area and 3% more power dissipating than that of wave-pipelined circuits.

1 Introduction

Wave-pipelining is one of the most complex techniques in VLSI design. As it is offering lot of advantages like less clock routing patterns, reduced delay rate, and less power consumption compared to pipelining techniques. Still, it challenges some of the underlying assumptions of the VLSI design movement of 80’s Cotten, as he mentioned in [1], that this technique provides maximal rate of pipelining. Here the longest and shortest path delay determines rate of flow of operation within the circuit. therefore, multiple computing waves or signal logic can flow through clock routine at once. Due to several internal components present on SOC(System-On-Chip) parameters like power consumption, latency clock logics, area occupancy, operation delay increases in order to avoid this problem a best alternative method of pipelining circuit is used i.e., wave-pipelining and whole processes is carried out by adjusting three schemes i.e., clock skew, path delay, clock period. In order to

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verify these constraints a dual-tree Dual-Tree Complex Wavelet Transformation is used to analyze the efficiency of the automation method. The organization of this paper were included with section 2 previous work, section 3 proposed model, section 4 implementation of dual-tree complex wavelet transformation with self-tuned wave-pipelined circuit, section 5 implementation results, section 5 conclusion.

2 Literature Study

Based on the previous paper [2][3][4][5] it seen that every paper has unique verification techniques like DWT, Dedicated AND gate with fast carry logic multiplier which directly estimating the parameters like low power consumption, and less area occupation with three adjustment schemes

Here in this paper, we can enhance the advanced technology in order to verify the constraints with a method called dual-tree complex wavelet transformation which is double comminated 2d DWT implementation

3 Proposed System

3.1 Design of Wave-Pipelined Circuit

As mentioned in the paper [2][3][4] a wave-pipelined circuit is a typical combinational logic circuit along with the input and output registers [5], and establish the timing requirements of wave-pipelined circuit for this configuration. Time limits at every individual stages separately in pipelined circuit whereas in wave-pipelined circuits all the timing and clock logic enable initially at once for multiple tasks. Several systems, including ASICs, FPGAs have been implemented via wave-pipelining technique to maximize the efficiency of digital circuits and increase the amount of utilization work time.

Here it is combined with input and output registers along with all the clock skews, clock period, based on the longest and shortest path delay the overall delay rate is collected from the Dmin and Dmax which is shown in figure below.

Total delay of the circuit is denoted as ‘delta’ respectively.

Fig. 3.1. wave-pipelined circuit

The shaded region of both Dmin, Dmax represents logic levels of the logic block vary with respect to time. the unshaded region depicts the stable duration of logic block in the system. Output register is considered into unshaded region thus it is taken greater than that of clock period in general the wave-pipelining circuit has (Dmax-Dmin) + clock overheads (hold time).

With these constraints the wave-pipelined circuits didn’t produce shaded portions in every stage due to this, it proof that it occupies less power consumed, high maximal rate of
speed of operation archived. the three parameters like clock skew, clock period, path delay was greatly adjusted.

Fig. 3.2. Shaded/unshaded sectorial Diagram of wave-pipelined circuit

ADVANTAGES OF WAVE-PIPELINED CIRCUIT
- Less Area Occupancy
- Low path delay
- Low power consumption

4 Working methodology

4.1 Implementation Of Dual-Tree Complex Transformation Using Bist

4.1.1 The Dual-Tree Complex Wavelet Transform

As shown in the previous Paper [6] it is the enhancement of DWT with additional properties called shift invariant, directionally selectivity of higher dimensions. DTCWT is a dual-tree CWT is non separable but is based on a computationally efficient, separable filter bank (FB)

4.1.2 Dual-Tree Framework

Dual-tree complex transformation is an analytic wavelet transform and introduced by Kingsbury in 1998, it is of positive/negative post-filtering of real sub-band signals, the dual-tree approach is quite simple. The dual-tree CWT employs two real DWT systems. in which the first DWT filters gives the transformation info of real part where as second DWT filter explains about imaginary part of transformation of the system. The implementational analysis and synthesis are shown in the below figures respective.

The two real wavelet transformation is the combination of two different real & imaginary part of various set of filters. the total response of the system can be collected from both the real and imaginary part of the filter functionalities respectively. Let \( h_0(n) \), \( h_1(n) \) are the real part of the lowpass/high pass filter pair for the lower filter bank. \( g_0(n) \), \( g_1(n) \) are the imaginary part of the
**Figure 4.1.** Analysis of FB’s for the dual-tree discrete complex wavelet transform (CWT).

**Figure 4.2.** Synthesis of FB’s for the dual-tree discrete complex wavelet transform CWT.

g₀(n), g₁(n) are the imaginary part of the lowpass/high pass filter pair for the lower filter bank. Here the two real wavelets associated with each of the two real wavelet transforms denoted as ψₕ(t) and ψₔ(t). In order to satisfy PR conditions, the filters are designed so that the complex wavelet as

\[
ψ(t) := ψₕ(t) + j ψₔ(t)
\]

where: ψₔ(t) is approximately replica the Hilbert transform of ψₕ(t), [denoted ψₔ(t) \( \approx H[ψₕ(t)] \)].
4.2 Designing of Filters of Real Wavelets Transform for The Dual-Tree Cwt

In order to design the filters of real wavelet transforms various approaches are employed in dual-trees CWT and they must satisfy the following conditional properties;
1. Satisfy half-sample delay Condition
2. Reconstruction conditions of orthogonal & biorthogonal
3. FIR filters
4. Filters to satisfy the Vanishing moments, stopband condition.
5. Filters should satisfy linearity in phase throughout the transformation

Here, the complex filter responses must be linear-phase; this can be achieved by taking

\[ g_0(n) = h_0(N - 1 - n) \]

Note: the entire work behind this topic was very clearly explained in previous papers [6][7].

4.3 Built In Self-Test Circuit Approach for Wave-Pipelined Circuit

For the purpose of tuning the clock frequencies and clocks with varying skews, it is recommended to use a BIST circuit within the wave-pipelined circuit itself. i.e Fig 3 is a block diagram of a pipelined Self Tuned Wave circuit.

The PRSG block, PRBS sequence generator, signature analyser, counter, Programmable Clock generator Circuit, Programmable skew generator Circuit, and Field-programmable Gate Array (FPGA) are few samples functional blocks which incorporate this system.

There are two distinct modes of operation for a self-tuned wave-pipelined: test mode and normal mode. The mode of operation is chosen by use of the TM signal. By setting the TM signal to 1 the circuit is put into test mode. First, the FSM provides a CS= 0 for the clock generator and an SS=0 for the skew generating circuit when in test mode. Those initial clock pulses is then distributed to the PRSG circuit, the programmable skew generating circuit, and the input register via the programmable clock generator circuit. For thorough testing, the PRSG building block is employed, which produces all $2^n$ possible inputs for an n-bit input.

The output register and counter receive a skewed clock from the configurable skew generating circuit. After all test vectors have been applied, the enable signal(sign) is generated by the counter, which keeps track of the number of test vectors provided to the combinational block. Instead of comparing each output to the predicted output, the PRBS generator creates a signature from the outputs corresponding to all the inputs and then compares this signature to a previously recorded value in the signature analyser circuit.

The signature analyzer communicates with the FSM block via two control signals, one of which indicates whether or not a match was found. CS, SS are the input values of clock, skew generator circuits were created based on control signal from the signature analyzer. When no match is found, the FSM will randomly swap the SS value between 0 and 7 for each CS value. If there is no match after applying all the skews to a given CS value, the CS value is modified. To do so, FSM iteratively varies the CS and SS parameters until a match is made. After a successful match is made, the FSM will set the CS and SS values and
return the circuit to normal operation by setting the TM to 0. In the default setting, users can apply their commands.

![Diagram of a Self-tuned wave-pipelined circuit.](image)

Figure 4.3. A Self-tuned wave-pipelined circuit.

### 4.4 Procedure Adjustment Steps of The Clock Period and Skew

The clock skew and period adjustments can be generated automatically with the help of implementing programmability, incorporating a programmable clock and clock skew generator is possible. Programmable clock generator is made up of a delay block and an inverter. In practice, Latency among connections gives the clock period. The choose input of the multiplexer can be select in between processor or a Finite State Machine (FSM) were a wide range of clock rates to be achieved. Similarity in the feedback linked circuits were deleted and the selection line changed through FSM to produce variable degrees of clock skew.

In order to operate the wave-pipelined circuit at a higher frequency it is possible with the available synthesis tools, i.e. D-max is used for fixing the operating frequency were the clock and skew generator can be programmed. Variable implementing the automation can be carried out by sectional option between both off-chip processor and on-chip processor. When the FPGA is acting as a hardware accelerator for a main CPU or FSM, the off-chip processor is used.
Communication between FPGA & Processor of off-chip is slower than that of on-chip. the time delay of clock frequency and skew are reduced among wavelet transforms with the use of built-in self-test approach which actually a design testability technique.

5 Conclusion

From this paper it is concluded that an automated wave-pipelined circuit is implemented with dual -tree complex transformation using ASIC and it is observed that wave -pipelined circuits are approximately 30% more faster than that of non-pipelining circuits, pipelined circuits are 49% more faster Than that of wave-pipelined circuits but occupies 30% more area and 3% more power dissipating than that of wave-pipelined circuits.

References