A large gain variable range, high linearity, low noise, low DC offset VGAs used in BD system

Dianwei Zhang[1, *], *Fei* Chu[2], *Wu* Wen[3], and *Ze* Cheng[3]

[1]Beijing Microelectronics Technology Institute .BeiJing, China
[2]Beijing Mxtronics Technology Co.Ltd, Beijing, China
[3]Beijing Microelectronics Technology Institute. Bei Jing, China

Abstract. In this paper, a large gain variable range, high linearity, low noise, low DC offset VGAs with a simple gain-dB variable circuit are introduced. In the VGAs chain, the last and the first VGAs employ Bipolar transistors, to improve the linearity and noise characteristics. And the middle three stages VGAs employ MOS transistors. The whole circuitry is designed in 0.35um BiCMOS process, including variable gain amplifiers (VGAs) , fixed gain amplifiers , gain control and DC offset cancellation parts. The automatic gain control loop (AGC) provides a process independent gain variable range of 60dB (including 50dB gain-dB-linearity variable range), with a 200us loop lock time, the VGAs provide a 73dB largest gain, the THD is less than 1% at a 1V(P-P) output level; the equivalent output integral noise is 0.011v/√hz@20MHz bandwidth. The whole area is 1173um*494 um, and the power is 7.1mA at 3.3V signal supply voltage.

Keywords: VGA, AGC, RF, ANALOG, SATELLITE NAVIGATION, dB-LINEARITY.

1 Introduction

VGAs are kinds of circuits that are very common in analog system. They are widely used in CCD, disk[1][2][3], acoustics[4][5], detector[6][7] and communication systems[8][9][10]. In communication systems, almost all type of RF frond end receivers need VGAs. And the VGAs are normally employed in a feedback loop to implement an automatic gain control amplifier. Fig.1 gives a kind of applications of VGAs in communication systems. However, all these systems which need VGAs have the same characteristic: the signal is weak and the signal power varies in a wide range.

Normally, there are several parameters of VGAs such as: gain variable range, dc offset rejection, gain control precision need to be carefully considered. For example: in the disk systems, the VGAs must have controllable gain range of 30dB [1]. In GPS systems, to consider all the uncontrollable factors a 40dB gain range is enough [11]. But in the BD system a more than 60dB gain range is needed. Also there are many other characteristics such as: gain – dB - linearity variable, low noise, high linearity, short loop lock time(if there is a AGC loop) need to be thought. In the second part we will discuss these characteristics.

* Corresponding author: zhangdianwei313@163.com

Now there are two focuses in VGAs application-field—the gain-dB-linearity variable circuit and the digital vgas. As we know, the CMOS process is becoming the mainstream technology. But in CMOS technology, the gain-dB-linearity variable circuits cannot be realized directly. So there are many methods: pseudo-exponential [12], various Taylor series approximation[13][14][15][16] are used to realize a exponential function. No matter which method to choose, all these realizations are aimed at improving the gain variable range in a dB mode with the control voltage. Also in recent years, since the DSP technology has gotten great development. And people begin to use DSP technology to realize traditional VGAs (in this case, VGAS usually are called PGAs: programmable gain amplifiers). To PGAs, the gain can change in any way, so the gain-dB variable circuits are not a problem. But the PGAs cannot give continuous variable gain, the designers optimize the gain discretely only. That may be a question in some systems.

In this paper, a large gain variable range, high linearity, low noise, low DC offset VGAs with a simple gain-dB-linearity variable circuit are introduced. In the second part, several important characteristics are discussed; in the third part, the VGAs , AGC and the gain-dB-linearity variable circuits are referred; in the fourth part the layout and test results are given; in the final part, a conclusion is made.

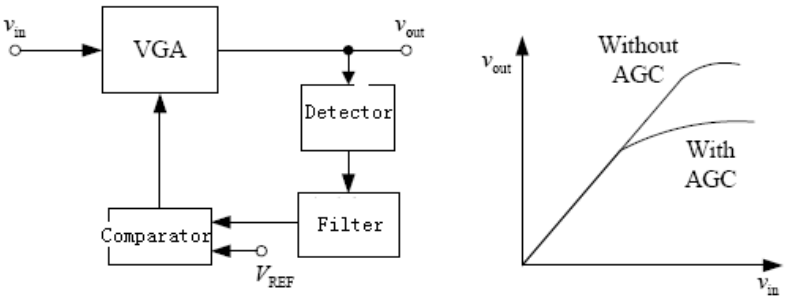

Fig. 1. The traditional architecture of AGC loop used in communication system.

2 The system design consideration

In the BD system, several parameters need to be carefully considered. The first one is the gain variable range. Not like other satellite navigation systems, the signal of BD systems has a wide variable range, so the VGAs must give a large controllable gain variable range to keep the output of IF signal at a fixed level (to alleviate the requirement of the ADC). But it is a challenge to supply a large gain variable range without cascade too many VGAs. Furthermore, the frequency of the IF signal is larger than 50MHz, so, too many cascaded VGAs will destroy the bandwidth. Just as Fig 2 displays the signal coming from the antenna may change 20dB and the gain of the RF Frond End circuits may vary 40dB. So, to consider all these possible factors of the system, the gain variable range should not be less than 60dB.

The second parameter is the high linearity. In all communication systems, distortion is the most important factor. The larger the signal levels, the larger the distortion becomes .So, to get less distortion, the signal level must be small. But in BD system, the largest signal get to the antenna is nearly -60dBm, the VGAs must keep a low distortion to insure that the baseband can calculate data correctly. In the design, a 1% THD is required when the output level of the VGAs are 1V (P-P).

The third important factor is low DC offset. To think about that the largest gain of the VGAs is about 73dB, the DC offset of the VGAs must be small or the following circuits of VGAs, even the VGAs themselves will be saturation. In the design, we employ two kinds of circuits to cancel the DC offset: a low pass filter and a large DC offset capacitor. As the

measurement proved that a low pass filter to decrease the offset that produced by the VGAs themselves is necessary.

The fourth factor is the loop lock time. The VGAs of the BD system used in a negative feedback loop, and the system requires the loop lock time must less than 1ms. To consider that the AGC loop should keep stabling under a more than 73dB largest gain so the capacitor of the loop must be large. But to get a short loop lock time, the capacitor should be small. However, when design a AGC loop one have to compromise between stabling and loop lock time. The requirements of the system are summarized in Table.1.

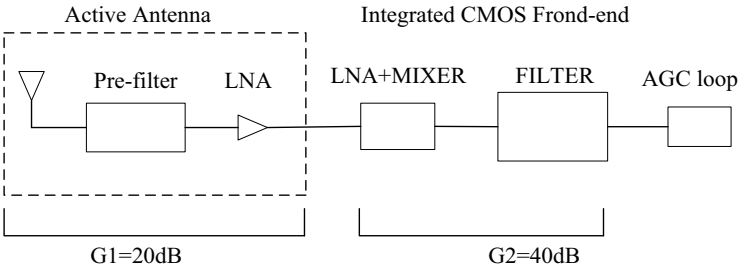

Fig. **2.** Gain variable of the RF Frond End of BD.

Table 1. The parameters of the VGAs used in BD system.

parameter	
Gain variable range	60dB
THD	<1% @1V(P-P)
Input noise	<10nV
Loop lock time	<1ms
DC offset voltage	<50mV@73dB gain

3 Circuits realization

3.1 The design of the VGAs chain

The block diagram of the AGC loop is depicted in Fig. 3. It includes three cascaded VGAs and a fixed gain buffer. The output of the fixed gain buffer is a full-wave rectified circuit, though a comparator and a dB-linearity circuit the gain-control voltage is filtered by a big capacitor. And to cancel the DC offset of VGAs themselves, a DC rejection circuits is designed, to cancel the DC offset coming from the frond circuits, a DC capacitor are also employed in the chain of the VGAs.

In the VGAs chain, the last and the first VGAs employ Bipolar transistors, to improve the linearity and noise characteristics. And the middle three stages VGAs employ MOS transistors. All the VGAs have the same architecture, in the following part we will introduce.

In the feedback loop, we design a DAC, so one can choose though the AGC or by the DAC to change the gain of the VGAs chain.

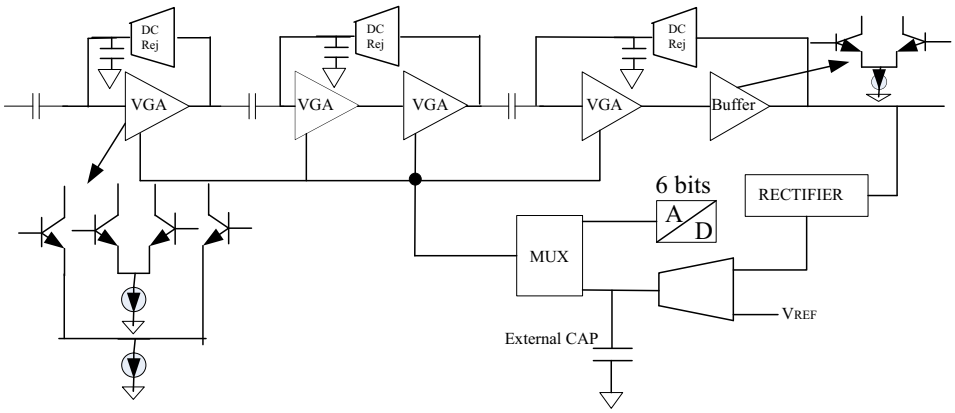

Fig. 3. Block diagram of the AGC loop.

3.2 The circuit realization of VGA

VGA is the core of an AGC loop. There are many prevailing VGA designs, and we can commonly group them into two types. One is to control the transconductance of the input transistors to change the gain, the other is to change the load of the VGA to change the gain. A great many circuitry realizations for analog VGAs also exist [2], and one of them is the use of analog Gilbert-multiplier cell [16]. The Gilbert-multiplier cell can provide wide bandwidth and excellent linearity characteristic. Fig.4 shows such a Gilbert cell in our VGA design.

In Fig. 4, the gain of the VGA is controlled by the bias current source. When the difference between Vcontrol1 and Vcontrol1 is small, the gain of the Gilbert-multiplier cell is little; otherwise the gain of the VGA is large. The gain of the VGA can be written as:

$$A_{vOut} = \frac{g_{m+} \bullet V_{in+} - g_{m-} \bullet V_{in+}}{V_{in}} \bullet R_{OUT} = R_{OUT} \bullet (g_{m+} - g_{m-}) \quad (1)$$

where the gm+ and gm- are the transconductances of the input transistors.

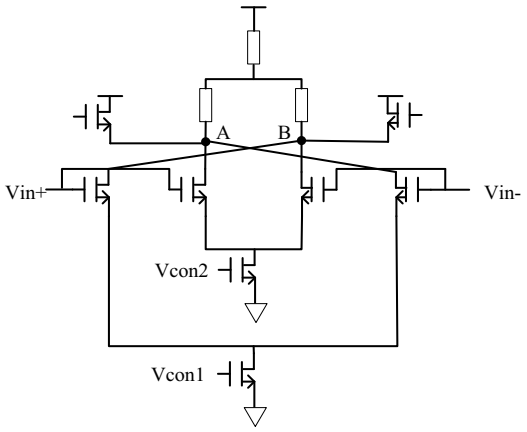

Fig. 4. Architecture of the VGA.

3.3 The circuit realization of the dB-linearity

In communication system, especially when the input signal variable in a wide range, such system need a gain-dB-linearity characteristic. In other words, these systems require a fixed loop settling time. Just take the BD system for an example to illustrate why these system need a gain- dB-linearity circuits to realize a fixed loop settling time.

In BD system, the signal coming from the antenna varies in a large range. So the settling time of the ACG loop will varies in a wide range. As we know, in satellite navigation system, signal amplitude acquisition during a preamble where the data is transmitted. The preamble duration should exceed the acquisition or settling time of the AGC loop. And its duration should be minimized for efficient use of the channel bandwidth. If the AGC circuit is designed such that the acquisition time is a function of the input amplitude, then the preamble is forced to be longer in duration than the slowest possible AGC circuit acquisition time. Consequently, to optimize system performance, the AGC loop settling time should well defined and signal independent.

The relation between gain-dB-linearity characteristic and a fixed loop settling time is a complicated issue. If we build a model of the whole AGC loop, and let the loop settling time independent of the signal amplitude then we will get a interesting conclusion: that the gain of the VGAs and the gain control voltage have a exponential function(2) . Readers who are interested in that may study reference [17][18].

$$\mathrm{A(v)} = \exp^{\mathrm{Vcontrol}} \tag{2}$$

In this paper, we use Taylor series to approximate the exponential. As we know, in (3) when x<<1, we can approximate the exponential function with the front several terms.

$$e^x = 1 + \frac{x}{1!} \tag{3}$$

The designed dB-linearity circuit is depicted in Fig. 5. Through these circuits we can get nearly 50dB gain variable range in a dB-linearity mode by four stage VGAs.

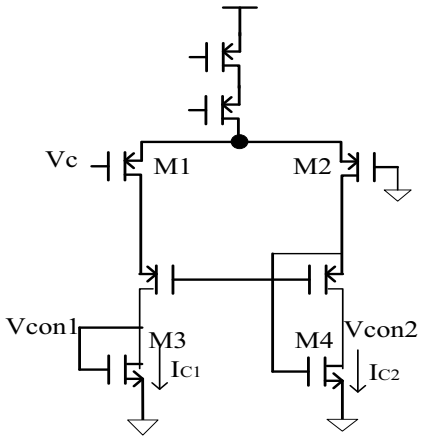

Fig. 5. Gain-dB-linearity circuits.

3.4 The design of AGC circuits

Fig.6 is the feedback control circuit. FWR-Sig is the output of the Voltage follower, Vref is a constant voltage level. The difference between FWR-Sig and Vref decide the signal amplitude of the AGC. The amplitude of the output of the AGC can be described:

Which A is amplitude of the output signal of the VGAs. In Fig.5 the total currents through M1, M2 are constant. The control voltages are the gates bias voltages Of M3 and M4. If the currents through the two transistors are equal, then the gain of the VGA is zero. Else if more current through M3 or M4, the gain of VGA will become larger. When the amplitude of the output signal meets the requirement of formula (4), the currents through M3 and M4 in Fig.6 will be constant, the whole AGC circuits get to a steady state.

$$\int_0^{\frac{\Pi}{\omega}} \frac{-A\sin wt}{\frac{\Pi}{\omega}} dt = FWR\_Sig - Vref \tag{4}$$

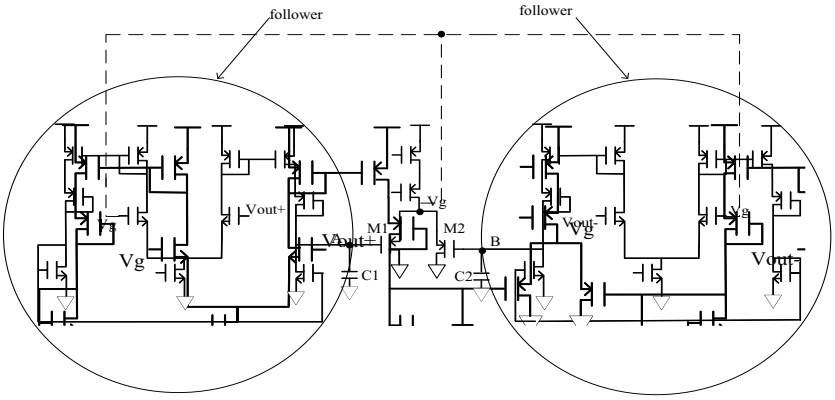

Fig. 6. The architecture of the full-wave-rejection circuits.

4 The layout and test result of the loop

Figure 7 is the picture of the whole RF Frond End Receiver. The layout of the whole AGC loop is depicted in Fig. 8. Because the IF is more than 50MHz, the layout should be compacted to reduce the parasitic capacitors and resistors. Fig. 9 is the picture of the evaluation kit.

The linearity characteristic of the VGAs is depicted in Fig. 10. As Fig.10 shows, even the signal level getting to the VGAs is -27dBm, the VGAs can correctly amplify the signal. Fig. 11 gives the frequency response of the VGAs. Fig.12 gives the gain dB-linearity variable range. Fig.13 gives the input noise density of the whole loop. Due to the first VGA employing bipolar transisitors, the input noise density is less than 4nV/sqrt(Hz). Table.2 gives the test results of the whole AGC loop.

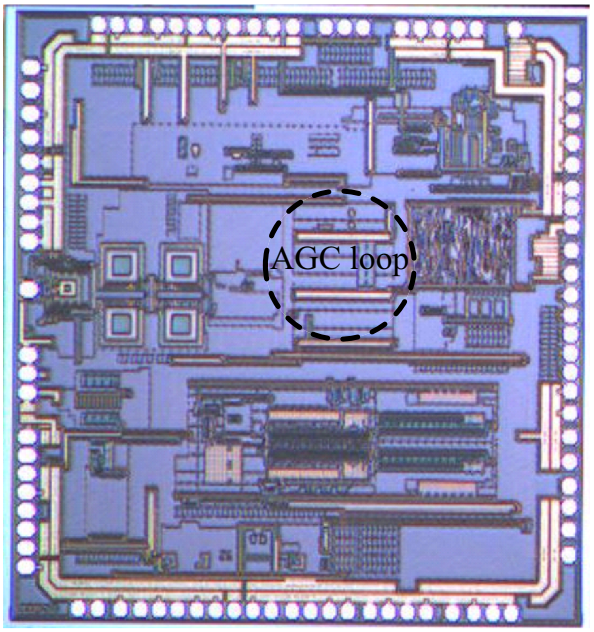

Fig. 7. The whole RF Frond End Receiver.

Fig. 8. The layout of the loop.

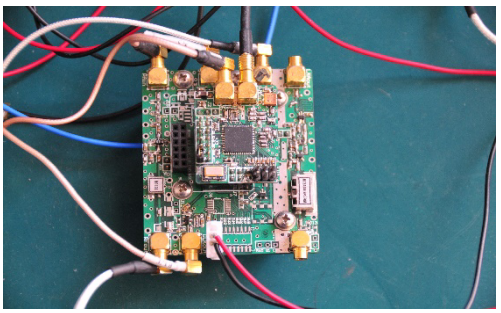

Fig. 9. The evaluation kit.

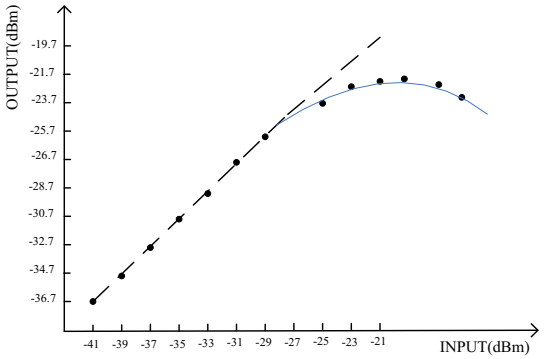

Fig. 10. 1dB compression point of the VGAs.

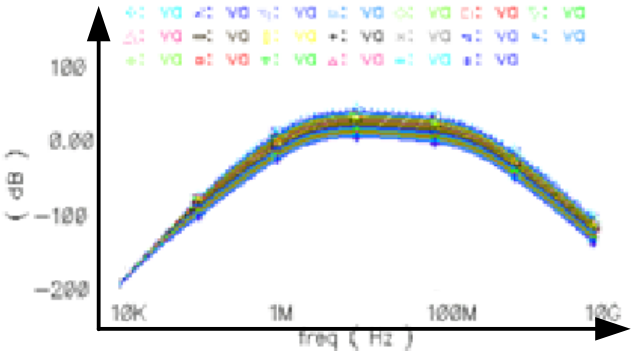

Fig. 11. Frequency response of the VGAs.

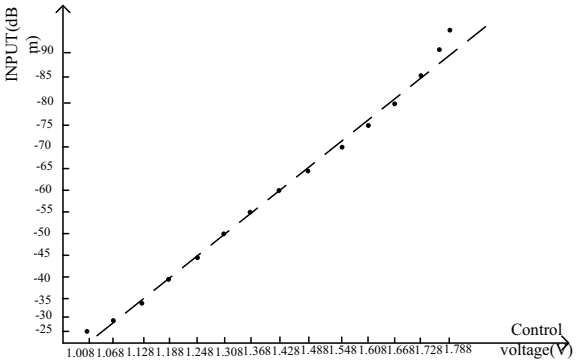

Fig. 12.dB linearity of the VGAs.

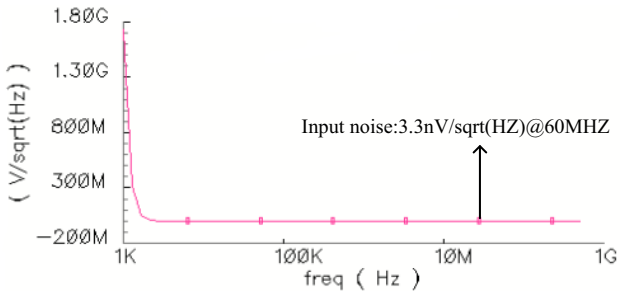

Fig. 13. Input noise density.

Table 2. Test results of the AGC loop.

	test
Input sig range	[-73dBm, -23dBm]
sig level(p-p, differential)	0.9V
DC offset rejection	<20mV@output@largest gain
dB linearity range	50dB
largest gain	73 dB
-3dB bandwidth	30M-56M
Input noise	<10nV
1dB compression point	-21 dBm@27dB gain; -71 dBm@80dB gain
Loop lock time	200us
power	7.1mA

5 Conclusion

In this paper, a high gain variable range, high linearity, low noise, low DC offset VGAs with a simple gain-dB variable circuit is introduced. The whole AGC loop has been used in the Bei Dou RF Frond End receiver. Test results show that the loop suits the system requirements.

References

1. “A 50-MHZ CMOS Variable Gain Amplifier for Magnetic Data Storage Systems” JSSC, 1992. R.Gone z, A.A.Abid
2. “A Low-Power CMOS VGA for 50Mb/s Disk Drive Read Channels” IEEE Trans, Circuits Sys, 1995
3. “A 95dB Linear Low-Power Variable Gain Amplifier” IEEE Trans, Circuits Sys, 2006. Quoc-Hoang Duong, Quan Le
4. “A Lower-Voltage Lower-Power Fully Integrated Automatic Gain Control for Hearing Instruments” JSSC, 1994. W.A.Serdjin, Van der Woerd, J. Davidse, and A.h.m.Van Roermund
5. “Multi-Channel Frond-End Readout IC for Position Sensitive Solid-State Detectors” IEEE, TU may o.Tumer, Victoria B.Cajipe.
6. “Integrated Readout Electronics: Enabling Advanced Applications of Position-Sensitive Solid-State Radiation Detectors” IEEE, 2004. Victoria B.Cajipe, Robert F.Calderwood.
7. ”A 71-MHZ CMOS IF-Basedband Strip for GSM” IEEE JSSC, 2000. Daolo Orsatti, Francesco Piazza, and Qiuting Huang

8. "Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver" JSSC, 2001. Farbod Behbahani, Ali Karimi-San jaani, Wee-Guan Tan, Andreas Roithmeier
9. "A Signal-Stage Variable-Gain Amplifier With 70-dB Dynamic Range for CDMA2000 Transmit Applications" JSSC, 2003. Sudhir Aggarwal, Abolfazl khosrowbeygi, Amd Auton Daaneninho Ko, Jongmoon Kim, Sanghyun Cho Lee "A 19-mW 2.6-mm L1/L2 Dual-Band COMS GPS Receiver" IEEE Journal of Solod State Circuits.Vol.40.No.7.July 2005
10. "Pseudo-Exponential Function for Mosfets in Saturation" IEEE Trans. Circuits, sys. 2000 Cheng-Chieh, Shen-Iuan Liu
11. "A 3.3-V CMOS Wideband Exponential Control Variable-Gain-Amplifier" IEEE 1998. Po-Chiun Huang, LiYu Chiou and Chorng-Kuang Wang
12. " A Temperature Stable CMOS Variable Gain Amplifier with 80-dB Linearly Controlled Gain Range"
13. 2001 Symposium on VLSI Circuits Digest of Technical Papers Takafumi Yamaji, Nobuo kanou, and Tetsuro Itakura
14. "A Low-Power Low-Noise Accurate Linear-in-Db Variable-Gain Amplifier with 500-MHA Bandwidth" JSSC, 2000. Shoji Otaka, Gaku Takemura, and Hiroshi Tanimoto
15. Behzad Razavi "Design of Analog CMOS Integrated Circuits"
16. "Improved Dynamic MODE of Fast-Settling Linear-in-dB Automatic Gain Control Circuit" Hsuan-Yu Marcus Pan and Lawrence E. Larson IEEE 2007
17. "On the Design of Constant Settling Time AGC Circuits" John M. Khoung, IEEE Trans. Circuits, sys. 1999