Design of multi-channel analog acquisition system based on DSP + FPGA architecture

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Abstract. This paper proposes a design and implementation of a general multi-channel analog acquisition system based on DSP + FPGA architecture. In terms of hardware architecture, FPGA is used to achieve high-speed and high reliability switching between different analog channels; FPGA + DSP data processing architecture is used to separate data acquisition and algorithm processing.

1 Introduction

Data acquisition is the basic means to obtain information. Analog quantity acquisition system can collect and process physical quantity to realize the monitoring or control of physical quantity. Based on 32 channels, this paper proposes a design scheme of multi-channel analog acquisition module based on DSP + FPGA, which has PXI bus interface module. The module uses advanced digital signal processor DSP as CPU, which can realize multi-channel analog signal scanning and acquisition, and has the characteristics of high precision, safety and reliability.

2 Overall system scheme

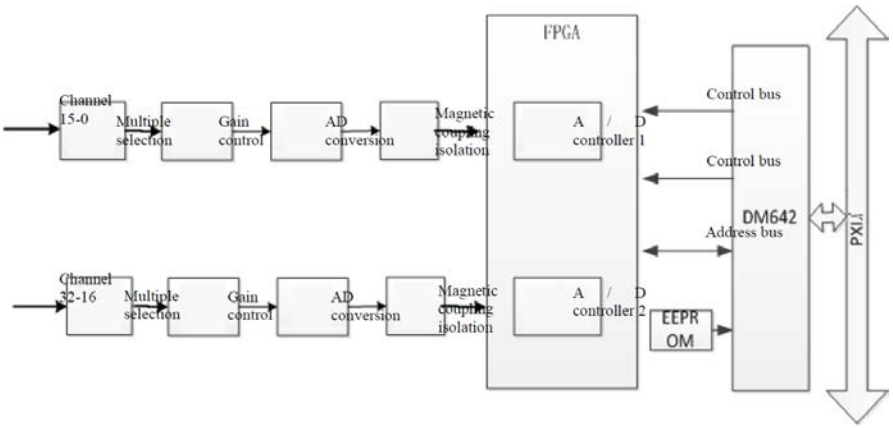

Fig. 1. General block diagram of 32-channel analog acquisition module.

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The overall scheme is shown in Figure 1. DM642 DSP is used as the main controller of the 32 channel analog acquisition module, and FPGA contains two groups of independent A / D controllers to control and process the two parts of a / D acquisition circuit respectively. The front-end analog circuit consists of multi-channel selection circuit, programmable gain circuit, a / D conversion circuit and magnetic coupling circuit.

3 Detailed design

3.1 Hardware circuit design

3.1.1 Multiplexer module

Multi channel analog switch is used to gate multi-channel signals to realize sequential scanning of multi-channel signals. The 32 input signals are divided into two groups, 16 in each group. The principle block diagram of multi-channel gating module is shown in the figure.

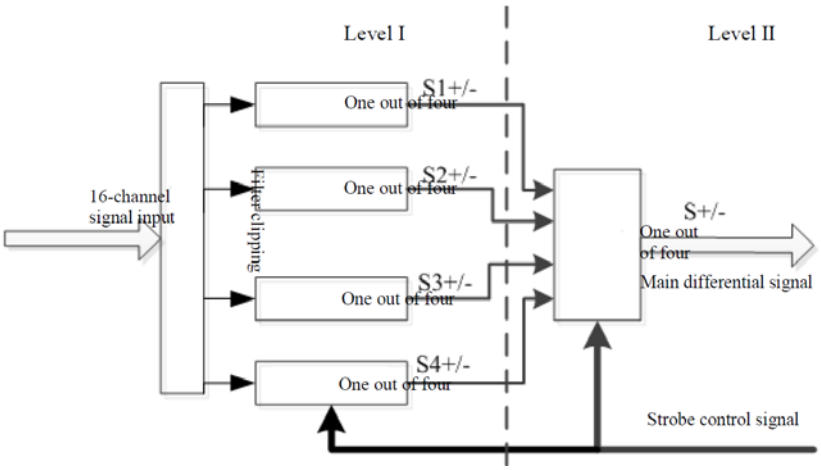

Fig. 2. Principle block diagram of gating module.

3.1.2 Signal conditioning module

The signal conditioning module is used for signal amplitude conversion and signal polarity adjustment to make the output signal meet the input requirements of the later stage AD conversion module.

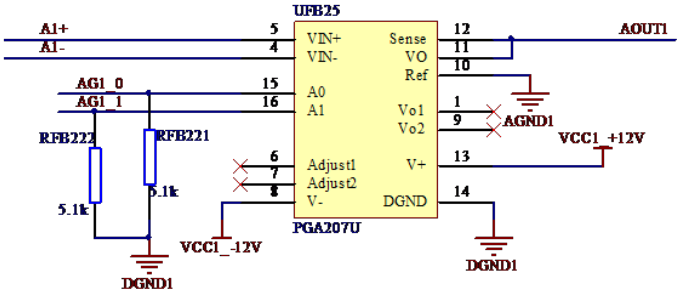

Fig. 3. Schematic diagram of differential single ended conditioning circuit.

3.1.3 AD Conversion module

The AD conversion module realizes the digital quantization of the analog signal and outputs the quantization result to the control module.

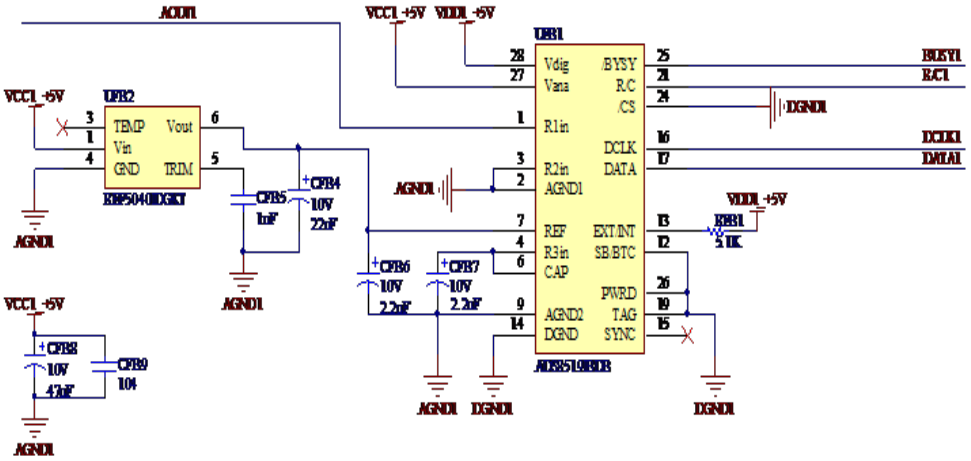

Fig. 4. Schematic diagram of AD acquisition circuit.

3.1.4 Signal isolation module

In order to ensure the isolation of the controller and the acquisition circuit, this design uses a digital isolator to isolate the input and output of the controller. The isolated signals include: analog switch control signal, PGA gain control signal, ad timing control signal and ad data acquisition signal.

3.2 FPGA control logic design

FPGA control logic is used to generate gating module control signal, PGA gain control signal, ad chip control signal, and provide internal FIFO to store the collected quantitative data of ad chip for upper processing. The internal logic block diagram of the module is shown in the figure.

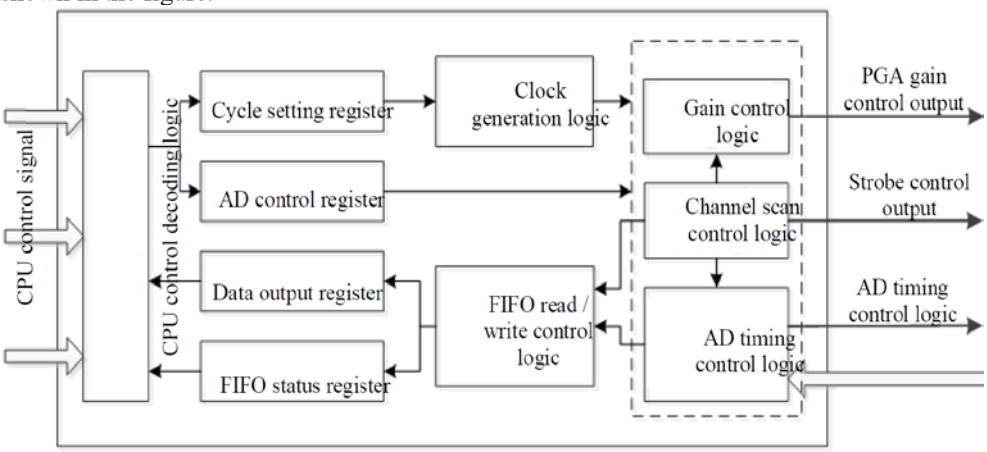

Fig. 5. Logic block diagram of FPGA control module.

3.2.1 CPU control decoding logic

The interface between CPU and FPGA is a standard three bus form: 16 bit data line + 16 bit address line + control line. CPU controls FPGA by reading and writing registers through bus access. The CPU control decoding logic decodes the register address that the CPU wants to access, and writes the control parameters into each control register of the FPGA internal module. The principle is shown in the figure.

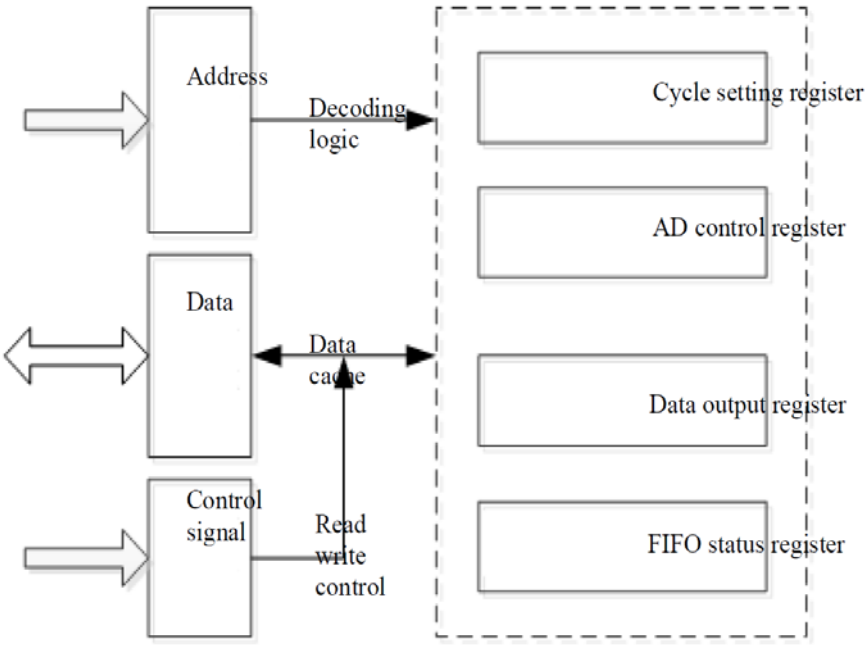

Fig. 6. Principle of control decoding logic.

3.2.2 Clock generation logic

Clock generation logic is used to generate the clock needed by FPGA internal logic and various clocks related to AD sampling. The input of the module is a 50MHz system clock, and the output has three kinds of clocks: the working clock of the module_ 12M_ CLK, sampling reference clock_ 20M_ CLK, sample_ clk.

3.2.3 Channel scan control logic

The AD acquisition system has 32 input channels, which are divided into two groups, 16 channels in each group. The channel scan control logic determines the scan channel range according to the configuration parameters of CPU.

3.2.4 Gain control logic

The main function of the gain control logic is to generate the corresponding PGA amplification control signal according to the current CPU configuration of the input range. According to the design requirements, the input range is divided into four levels: ± 1V, ± 2V, ± 5V, ± 10V. The corresponding PGA magnification is: 10,5,2,1.

3.2.5 Ad timing control logic

The ad timing control module is used to generate the control signal of ad chip and read back the acquisition result.

3.2.6 FIFO read / write control logic

FIFO read-write control logic is used to store and read the data collected by AD. According to the design requirements, each channel needs 8K storage depth, so the whole module includes 32 8KB FIFOs. The schematic diagram of FIFO read / write control logic is shown in the figure.

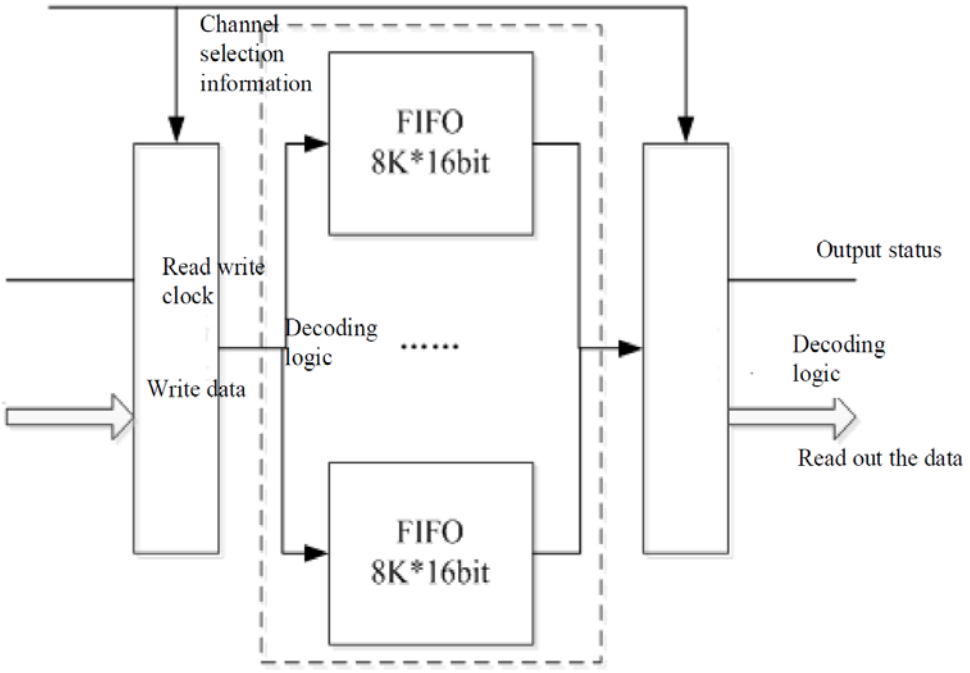

Fig. 7. Schematic diagram of FIFO read / write control module.

3.2.7 Register group

Register group is used to receive configuration parameters passed by CPU and return data and other status collected by ad to CPU. So the registers are all 16 bits, and the CPU operates them through the address corresponding to the register.

3.3 DSP program design

DSP program design is the key part of counter module software design, which has the function of realizing bottom communication and data transmission management.

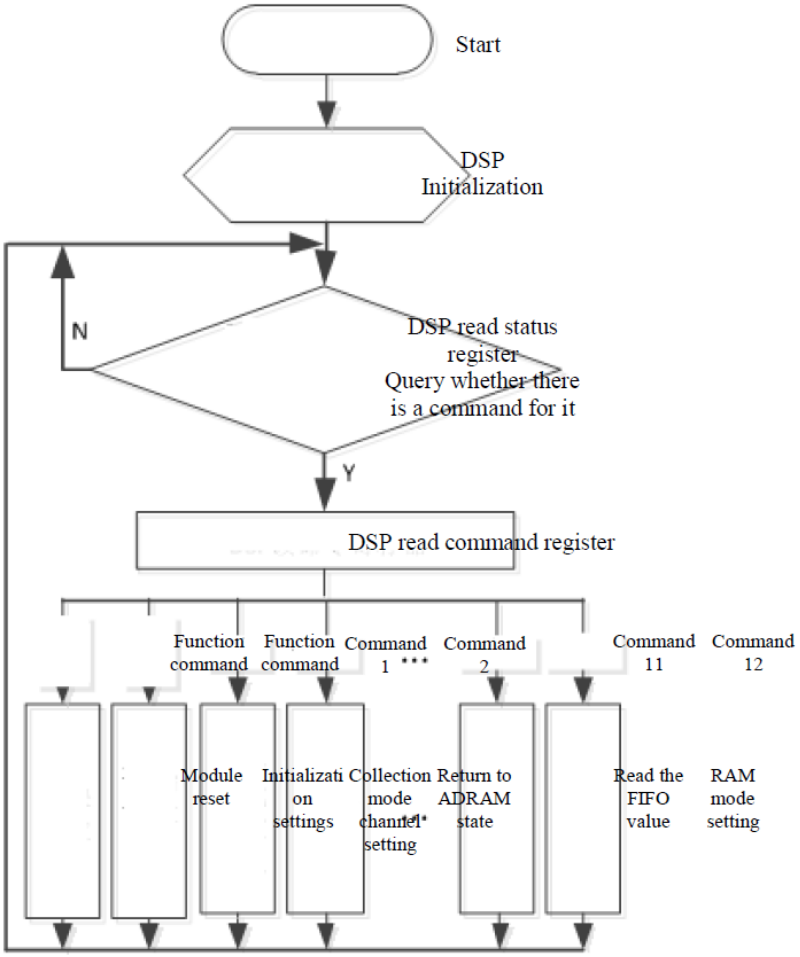

Fig. 8. DSP program execution flow chart.

4 Conclusion

The multi-channel analog data acquisition system based on DSP + FPGA adopts modular design to realize high precision and high real-time acquisition of multi-channel analog data. The system is easy to build, easy to expand, the reliability and real-time of the system has been greatly improved, and has a good application prospect.

References

1. Ma Mingjian, Data Acquisition and Processing Technology [M]. Xi'an, Xi'an Jiaotong University Press, 2005.