

# Digital NBC Protection System BIT Optimization Design

Li Guangsheng<sup>1</sup>, Ou Bo<sup>2\*</sup> and Wang Jianyuan<sup>3</sup>

<sup>1</sup>Li Guangsheng(1972-),male,Anqiu,Shandong Province,China, Associate Professor , mainly engaged in the research on detection technology and automatic equipment

<sup>2</sup>Ou Bo (1995-), male, Changde City, China, Master graduate student, mainly engaged in the research on detection technology and automatic equipment

<sup>3</sup>Wang Jianyuan (1994-), male, Wu xi City, China, Master graduate student, mainly engaged in the research on detection technology and automatic equipment

**Abstract.** BIT technology is an important means of system and equipment fault detection, location and isolation. This paper takes the digital NBC protection system as the research object, and carries out research on the optimization design based on BIT technology. Based on the structural division of the digital NBC protection systems and the analysis of typical failure modes, combined with the weighted cost index function and the selection method of the improved special hierarchically optimized optimal test set, the calculation and comparison of the indices of the actual digitalized NBC protection systems was conducted. Determine the optimal test set, and finally design the BIT circuit for the selected optimal test set.

## 1 Introduction

BIT testing technology is a new online fault detection technology that improves system reliability and reduces maintenance costs. It implements fault self-diagnosis of system circuits and key hardware units through hardware and software test units attached to the system [1]. The perfect BIT design can quickly and effectively detect, locate and isolate system faults, thus reducing maintenance and support links and saving manpower and material resources. In the field of weaponry, there are many successful applications for in-machine testing.

As the digitization and informatization process of armored equipment continues to accelerate, the proportion of numerical control subsystems in the electrical systems of armored vehicles is increasing, Online status detection and fault diagnosis have gradually become the main content of online fault diagnosis technology for electrical systems. With the application of more and more new power electronic devices and integrated circuits, there are many new problems in the fault detection and diagnosis of digital electrical subsystems. To this end, this paper selects the three-proof control system as the research object, and combines the completed digital three-proof controller design to carry out the research on the online fault diagnosis scheme of BIT technology.

## 2 Common BIT design methods and their advantages and disadvantages

At present, the more general BIT design methods for CNC systems mainly include Redundancy BIT, Surround

BIT, Parallel BIT and digital BIT based on boundary scan .[2]

### 2.1 Redundancy BIT

The redundancy BIT realizes the fault diagnosis of the circuit to be tested based on the comparison of the output results of the two sets of circuits by increasing the redundancy of the same function as the circuit under test. The online fault diagnosis based on the redundancy BIT has the advantages of not affecting the normal operation of the system and easy to implement the fault isolation function, but the design cost is high, and is usually used for fault diagnosis of key components.

### 2.2 Surround BIT

Surround BIT is widely used in the functional fault detection of microprocessor-based system peripheral hardware modules. It adopts the way of increasing the detection circuit and the hardware unit under test to form a loop, and implements the excitation through the processor I/O or other interfaces to judge the test loop response result, thereby realizing the fault detection of the hardware unit to be tested. Surrounding BIT has the advantages of simple principle, flexible design and low cost, and has a good application prospect in the numerical control electrical subsystem of armored vehicles.

### 2.3 Parallel BIT

Parallel BIT means that the system performs fault detection of the circuit and hardware unit under test while performing normal control functions. It has the advantages of simple BIT circuit design, low development cost and low system resource consumption.

\*Corresponding author: 707370034@qq.com

The disadvantage is that the trigger of its detection function is limited by the system control timing.

### 2.4 Digital BIT based on boundary scan

The digital BIT design based on boundary scan is a fault detection method for integrated electronic devices. With the boundary scan structure built into the device under test, the system controls the boundary scan controller to implement online detection of faults such as static functions and line connections. Compared with other BIT design methods, the digital BIT based on boundary scan can break through the physical access restrictions, and has the advantages of wide test range and high standardization. However, the BIT design cost is high, and the acquisition of electronic devices with a boundary scan structure also has certain difficulties.

### 3 Selecting the optimal test set based on the improved special hierarchical optimization method

By analyzing the functional structure characteristics of the digital three-proof system and the above BIT design method, combined with the typical failure mode table of the digital three-proof system, the system fault alternative test set shown in Table 2. is designed. Table 1.shows the typical failure modes of the digital three-proof system.

**Table 1.** Typical failure mode of digital three-proof system

Mode number	Fault description	Mode number	Fault description
$f_1$	Electric squib detonation circuit open circuit failure	$f_7$	External D/A chip is working abnormally
$f_2$	Fan working circuit function failure	$f_8$	Chip link failure
$f_3$	Atomic signal processing circuit works abnormally	$f_9$	Poison sensor open or shorted
$f_4$	Atomic signal sensor open or short circuit fault	$f_{10}$	Poison signal processing circuit works abnormally
$f_5$	Electric squib drive circuit failure	$f_{11}$	Fan working circuit parameter failure
$f_6$	Power system supply voltage overrun	$f_{12}$	Alarm circuit failure

**Table 2.** Digital three-proof system fault alternative test set

number	Test description method	Cpi	Csi
$t_1$	Surrounding BIT test electric squib detonation circuit open circuit failure	0.2	0.1
$t_2$	Surround BIT test atomic signal processing circuit function abnormal fault	0.2	0.1

$t_3$	Residual BIT test electric squib detonation drive circuit failure	0.3	0.1
$t_4$	BIT test poison signal processing circuit function abnormal fault	0.3	0.1
$t_5$	Test signal sensor open circuit, short circuit fault based on constant current surround BIT method	0.35	0.3
$t_6$	System self-test (does not increase test hardware, is controlled by MCU)	0	1
$t_7$	Parallel BIT test alarm circuit failure	0.15	0.2
$t_8$	Control power supply +5V output design over limit indication circuit, panel indication fault detection	0.1	0
$t_9$	Parallel BIT test electric squib detonation drive circuit failure	0.2	0.1
$t_{10}$	Surround BIT test fan loop function failure	0.35	0.5
$t_{11}$	Surround BIT test chip works abnormally	0.15	0.4

Based on the specific correspondence of each fault detection method in the alternative test set shown above, a typical fault mode set of the three-prevention system is established. Correlation matrix between F and candidate set T [3].

$$F-T = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix} \tag{1}$$

F-T number of rows in the matrix  $m=11$ , Corresponding test methods in the alternative test set  $t_1 \sim t_{11}$ , Matrix row vector corresponds to Boolean vector  $A = (a_1, a_2, \dots, a_{11})$ ; Number of columns  $n=12$  Corresponding to the typical fault mode set  $f_1 \sim f_{11}$ .

According to the literature review, the preferred indicators of the digital three-proof system test set are as follows: FDR indicator is 100%; Minimum test set lower limit  $N_{min}=7$ ; Weighted cost indicator function weight  $\alpha = 0.25$ , Solved by the minimum test set, Cooperating F-T is:

$$f = a_1 a_2 a_3 a_4 a_8 + a_4 a_6 a_8 a_9 a_{11} + a_1 a_2 a_4 a_9 a_{10} + a_1 a_4 a_6 a_8 a_{10} + a_4 a_6 a_8 a_{10} a_{11} \tag{2}$$

The above formula shows that The number of tests in the minimum test set  $T N_s=5$ ; The minimum test set in set  $A(TM)$  consisting of the smallest test set  $T_m$  in  $T$  is also

5 Obviously because of  $N_s < N_{min}$ , In order to achieve a better overall effect of the preferred test set, Introducing relaxation factor  $\zeta=1$  to determine the set  $A(T_m^*)$ , Using row vector increment 1 instead, Replace a4 in f with a5a7 get expression  $f^*[4]$ , The same as f, consisting of 5 or items, can be expressed a

$$A(T_m^*) = \{ (t_1 t_2 t_3 t_5 t_8); (t_1 t_2 t_3 t_7 t_8); (t_5 t_6 t_8 t_9 t_{11}); (t_5 t_6 t_8 t_9 t_{11}); (t_1 t_2 t_5 t_9 t_{10}); (t_1 t_2 t_7 t_9 t_{10}); (t_1 t_5 t_6 t_8 t_{10}); (t_1 t_6 t_7 t_8 t_{10}); (t_5 t_6 t_8 t_{10} t_{11}); (t_6 t_7 t_8 t_{10} t_{11}) \} \quad (3)$$

Express each test set in  $A(T_m^*)$  that has been listed as  $T^*_{m1} \sim T^*_{m10}$ , Weighted indicator function:

$$f(\sum C_{P_i}, \sum C_{S_i}) = \sum C_{P_i} + 0.25 \sum C_{S_i} \quad (4)$$

Calculated as shown in Table 3.

**Table 3.** Weighted cost indicator calculation result table.

Test set $T^*_m$	$T^*_{m1}$	$T^*_{m2}$	$T^*_{m3}$	$T^*_{m4}$	$T^*_{m5}$
Cost indicator $f(T^*_m)$	1.91	1.62	1.68	1.84	1.45
Test set $T^*_m$	$T^*_{m6}$	$T^*_{m7}$	$T^*_{m8}$	$T^*_{m9}$	$T^*_{m10}$
Cost indicator $f(T^*_m)$	1.93	1.89	1.54	1.71	1.48

Compare the above 10 sets of test set weighted cost indicator function values: Test set  $T^*_{m5}$  weighted cost indicator function has the smallest value,  $f(T^*_{m5})=1.45$ . Therefore, the optimal test set of the typical three-defense control typical fault mode set is  $T^*_{m5}$

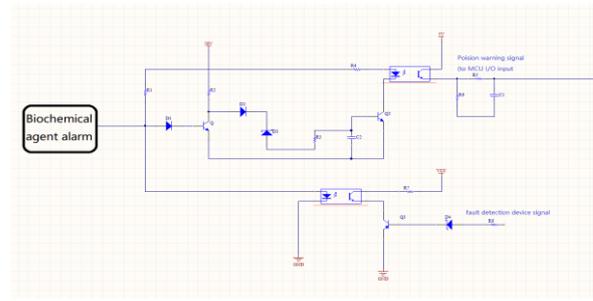
$$T_s = (t_1 t_2 t_5 t_9 t_{10}) \quad (5)$$

## 4 System BIT specific design

According to the previous section, analyze the typical fault set for the digital three-proof system F, the most alternative optimal test set is TS, Select a typical test method from it, Optimal test set  $T^*_{m5}$  is  $(t_1, t_2, t_5, t_9, t_{10})$ . This section will give specific design BIT design methods and simple principles.

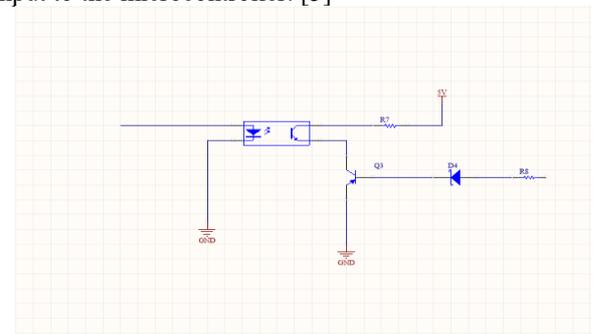
### 4.1 Detection design of poison alarm signal and nuclear alarm signal processing circuit around BIT

The BIT circuit is mainly designed for t2, and uses a surround BIT-based design method to detect the signal processing circuit. The specific circuit design is shown in Figure 1.



**Fig. 1.** Caption of the Figure 1. Below the figure.

According to the test analysis, these two signals are 24V voltage signals, and after modification, they are connected with the digital three-proof control box. Therefore, during this period, it is necessary to add and reduce the signal processing circuit, and the processed small signal is used as a dangerous situation alarm signal, that is, the core control chip I/O input. The surrounding BIT circuit designed in this section is responsible for detecting its signal processing circuit in real time. If the signal processing circuit fails, it is impossible to locate the fault location instantaneously on the signal sensor or the fault occurs on the signal processing circuit. Therefore, the test circuit is selected. The following is a brief description of the principles that enable real-time detection: When the core controller outputs a fault detection enable signal, Simulate the current nuclear pollution signal or chemical biological pollution signal by the surrounding BIT test circuit shown in the figure, the voltage signal of 24V, If the function of the nuclear pollution signal processing circuit is normal, the signal must be detected by the I/O input terminal of the core controller; otherwise, if the nuclear pollution signal processing circuit has a malfunction, it cannot be detected by the core control chip, Through this logic, if there is a fault point, the fault point can be successfully located. In the non-wartime use, in order to improve the accuracy of the detection, the general operation flow is to input the multiple-time detection enable signal, and determine the fault state based on the multiple diagnosis results. Figure 2. shows the surround BIT test circuit, Since the alarm is issued with 24V voltage, it cannot be directly input to the MCU. Therefore, the key function of the surrounding BIT test circuit is the step-down effect. Separated by optocoupler isolators, stepping down to the signal voltage input to the microcontroller. [5]



**Fig. 2.** Surround BIT test working diagram

## 4.2 Atomic pollution alarm exposure meter and poison alarm circuit state detection BIT design

According to the theoretical analysis, the condition monitoring of the alarm illuminometer based on the constant current surrounding BIT circuit should be designed, mainly for . However, starting from the actual situation, the nuclear alarm exposure meter equipped with the equipment now has the function of self-detection, and can display the state of the required detection on its own instrument. So the article does not describe the design circuit here, and only needs to transmit the detected state information to the core control chip to form a unified management of the state detection amount. Now explain the principle of self-testing and satisfying the state quantity information we need: According to the actual situation, the alarm illumination meter is hoisted on the top deck in front of the cab, there is a test alarm time jack, socket ,” Source check”and “Hand check” button on the panel. The most important is the source and the irradiation shutter linkage mechanism used in the movement's own self-test circuit. The workflow is briefly described as follows: The  $\gamma$ -ray receives a current pulse output from a detector element that receives the alarm circuit. The number of pulses output is proportional to the amount of  $\gamma$ -ray exposure, When the exposure reaches a certain rate, it is a dangerous situation. Then the corresponding output pulse is integrated and divided into a certain voltage of the circuit, Then trigger the working circuit to reach the alarm, so that the alarm indicator on the instrument can be illuminated. At the same time, the detection element ionization chamber of the measurement display circuit also outputs electric charge. The amount of charge varies with the amount of  $\gamma$ -ray irradiation, that is, the amount of accumulated  $\gamma$ -rays can be directly indicated by the counting of the digital tube. And now the amount of state I need to get is that is the working circuit for detecting  $\gamma$ -rays in good condition, Popularly speaking, its role is the role of a sensor signal. What is needed now is to detect the quality of the sensor signal. The source detection function is because the exposure meter comes with a  $\beta$  source irradiation shutter. In this way, the  $\beta$ -ray can be irradiated to the counter tube instead of the  $\gamma$ -ray irradiation by pressing the source detection function button without  $\gamma$ -ray, so that the self-check function for receiving the alarm circuit and the detection circuit function can be realized.

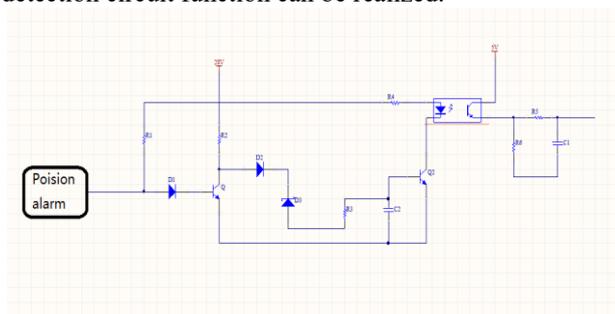


Fig. 3. Signal detection schematic.

Compared with the atomic signal alarm illuminometer, the chemistry agent alarm does not have such a self-test system, so it is necessary to add a BIT circuit to monitor real-time status information. The designed BIT circuit is as shown in Figure 3, A simple RC circuit is used between the poison alarm and the optocoupler isolator to form a double T circuit. The role played by the filter is to make the signal input to the microcontroller more stable after the final step-down. [6]

## 5 Conclusion

With the continuous upgrading of weapon equipment system, the application of BIT technology enhances the reliability of equipment. This paper first introduces four common BIT design methods and analyzes their advantages and disadvantages. According to the structural characteristics and functions of digital NBC protection system, referring to its typical failure mode, using the improved special hierarchical optimization method, summarizing the normalized test cost and test resource cost of each fault detection method in the test set , and then the optimal test set is determined by the weighted calculation of each index. Finally, for the selected optimal test set, the BIT design of the poison alarm signal and the nuclear alarm signal processing circuit in the NBC protection system is carried out, and the BIT design of the atomic pollution alarm exposure meter and the poison alarm circuit state detection is carried out. The circuit design of BIT is completed in theory, which provides reference for the BIT design of other digital systems.

## References

1. Yulan Zhang, Yongcheng Xie. Armored vehicle electrical and electronic systems[M]. Beijing, National Defense Industry Press, 2003
2. Shihua Geng, Weiwei Jiang, Qingsong Qin. Design and application of self-testing BIT technology in airborne equipment [J]. Information technology and information technology, 2017.4
3. Tianyou Wu, Design and development of intelligent evacuation indication system [D]. Hunan University, 2014
4. Xiaoyan Ma. Research on Testability Prediction Technology of Complex Electronic Equipment Based on Simulation Analysis [J]. Environmental technology, 2016.5
5. Wei Kuai. Optimized selection of test points [J]. Electronic test, 2012.2
6. Minjie Du, Jinyan Cai, Limin Liu. Optimized allocation of electronic equipment test resources for comprehensive diagnosis [J]. Electro-optic and control, 2013.1