Design of Digital Logical Controller in the Non-Circulating DC Speed Adjusting System

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Abstract. The non-circulating DC speed adjusting system is widely used. DLC is the core controller of the non-circulating DC speed adjusting system. The working principle of DLC was analyzed. A simulation model of the DLC controller was built. The parameters of the DLC were set. The reversible system obtained forward and reverse waveforms was obtained. And the simulation results surface: the method is correct and feasible.

1 Introduction

When the transition process of the process system does not require high smoothness, from the perspective of production reliability, a loop-free reversible system with neither a DC average circulation nor instantaneous pulsation is used. In production practice, the non-circulating DC speed adjusting system is often used. And the digital logical controller (DLC) is the core element of the non-circulating DC speed adjusting system. U^*_i and U_{i0} are the input signals of the digital logic controller, and the output signal contains the corresponding positive or reverse group rectifier bridge [1]. The circuit is composed of a level detecting circuit, a logic judging circuit, and a delay circuit. When the circuit works, the circuit sets reasonable parameters according to the actual situation to provide conditions for the correct implementation of the system [2].

2 Working principle of the DLC

The task of the logic loopless controller is to block the reverse group pulse when the positive thyristor is working, and block the positive group pulse when the reverse group thyristor works, and fundamentally cut off the circulation path.

To properly turn on the forward and reverse group pulses, the requirements for a logic loopless controller are as follows:

1. A logic switching command is issued jointly by the torque polarity signal and the zero current detection signal. When the torque polarity changes and the zero current detector sends a zero current signal, it is allowed to block the original working group and open another group.

2. After the switching instruction is issued, the original conduction group pulse must be blocked after the blocking delay time; after another open delay time, another group of pulses can be opened.

3. In either case, the two sets of thyristors are absolutely not allowed to add trigger pulses at the same time. When one group is working, the other group of trigger pulses must be blocked.

The DLC determines the logic state of the output based on the input of the controller. The two output signals of the logic controller respectively control whether to generate or block the trigger pulse through the flip-flop. The state of the output signals must always be reversed to ensure that the two sets of rectifiers are not operating at the same time [3].

The two input signals U^*_i and U_{i0} of the logic controller are important conditions for the logic controller to discriminate the state of the output signal. Both the braking of the motor and the changing of the steering require a change in the torque direction of the motor. The direction of the current in the system control is determined by the polarity of the speed regulator output U^*_i. Therefore, the symbol change of U^*_i is one of the conditions for the logic controller to switch [4].

However, the fast braking or reversing process of the reversible system has to undergo three stages of the bridge inverter, feedback braking and feedback braking. When the motor current drops to zero in the bridge inverter, the system experiences a reverse current in the reverse braking phase. If the rectifier is turned off when the bridge inverter has not ended, the inverter failure may occur and the rectifier may be damaged. Therefore, after the output of the speed regulator U^*_i changes polarity, it must wait for the current in the original direction of the motor to decrease to zero before the original rectifier can be turned off, thereby opening another set of rectifiers that were originally blocked. Therefore, the armature current U_i drops to zero, which is the second condition of the logic switching.

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Therefore, the output state of the logic controller can only be changed after U^*_i changes polarity and U_i=0.

3 Input and output logic control table of the DLC

The DLC establishes a simulation module based on the logical relationship between input and output in various operating states of the reversible speed control system. The relationship between logic controller inputs and outputs is shown in Table 1.

Table 1. Logic controller input and output relationship.

Signal state Operating status		Input		Output	
		U^*_i	Ui	U_{blf}	U_{blr}
Positive starting zero current		>0	0	0	1
Positive starting current and positive current		>0	>0	0	1
Positive braking	The bridge inverter has current	<0	>0	0	1
	The bridge inverter zero current	<0	=0	1	0
Reverse zero current		<0	=0	1	0
Reverse starting current and reverse current		<0	<0	1	0
Reverse braking	Bridge inverter has current	>0	<0	1	0
	Bridge inverter zero current	>0	=0	0	1

In Table 1, U^*_i>0 indicates forward torque, U^*_i<0 means reverse torque, U_i>0 means forward current, U_i<0 means reverse current, Ui=0 means zero current, U_{blf}=0 means the positive group rectifier works, U_{blf}=1 indicates that the positive group rectifier is blocked. U_{blr}=0 means the reverse group rectifier works, U_{blr}=1 indicates that the reverse group rectifier is blocked.

Through the analysis of Table 1, the logical control truth table is obtained, as shown in Table 2.

Table 2. Logical control truth table.

U_T	U_I	U_F	U_R
1	1	1	0
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	0	0	1

4 The composition of the logic controller

The logic controller consists of the following four parts: level detection, logic judgment circuit, delay circuit, and interlock protection circuit. The specific simulation circuit diagram is shown in Figure 1.

The function of the level detection circuit is to convert the input analog signal into a digital signal. The conversion is implemented by two hysteresis control modules. The conversion requirements are as follows:

1. Conversion polarity detection: when U^*_i>0, U_T=1, when U^*_i<0, U_T=0.

2. Zero current detection: when there is current U_i is not zero, U_I=0; when the current U_i is zero, U_I=zero.

The logic is composed of NAND gates YF1~YF4 whose inputs are torque polarity and zero current signals U_T and U_I; the outputs are logic switching signals U_F and U_R. The expressions of U_F and U_R are shown in equation 1 and equation 2.

$$U_F = \overline{U_R\left(\overline{U_T U_I}\right)} \tag{1}$$

$$U_R = \overline{U_F\left[\left(\overline{U_T U_I}\right)U_I\right]} \tag{2}$$

After the logic judgment circuit issues a switching instruction, the rectifier operating state cannot be changed immediately. The reason is as follows: When the detection current is zero, the armature current does not necessarily reach zero, and it must be delayed by about 3 milliseconds to ensure that the current is really zero, and then the command can be issued to turn off the turned-on rectifier. And in order to ensure that the cut-off rectifier can resume the blocking state, the open rectifier needs to be delayed for a period of time and then open, and the

open delay is generally about 7 milliseconds. The turn-off delay and open delay are generated by a delay circuit in the logic controller. In addition, there is no need for a delay on the falling edge of the signal.

For the interlock protection circuit, in normal operation, the two outputs of the logic judgment and delay circuit are always one "1" state and the other is "0" state. In the event of a fault, both outputs and if they are in the "1" state at the same time, will cause both sets of thyristors to open at the same time, causing a short circuit in the power supply. In order to protect the positive and negative sets of rectifiers from simultaneous opening, the NAND gate consists of an interlock protection circuit. The NAND gate is used because the levels of the outputs U_{blf} and U_{blr} are consistent with the level requirements of the block terminal of the trigger unit. When both U_F and U_R are "1", both sets of rectifiers are turned off to avoid rectifier short-circuit faults.

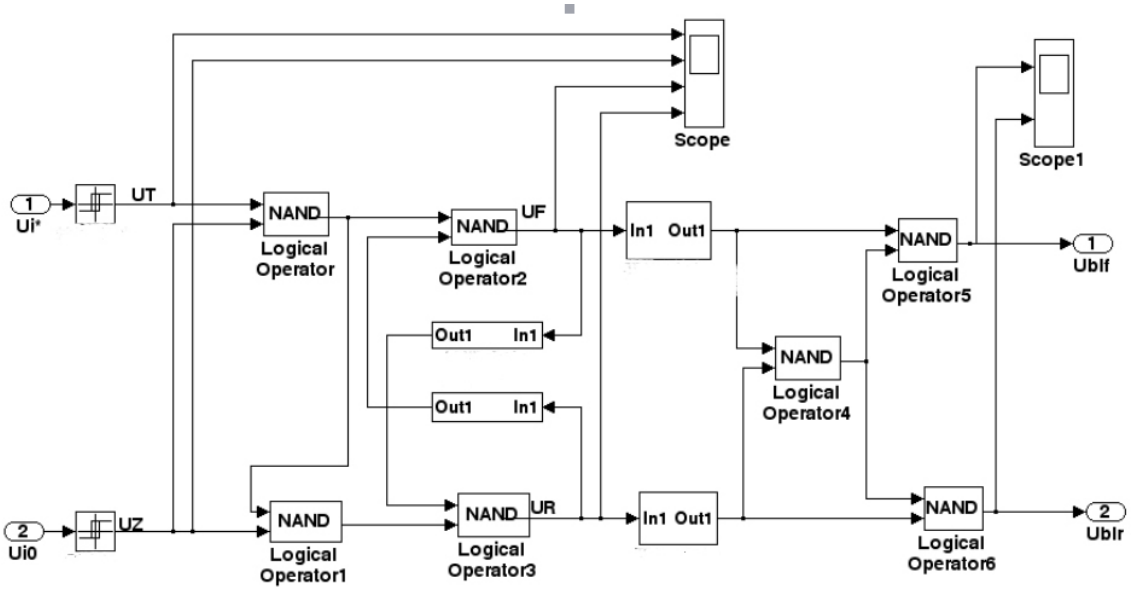

Figure 1. Logic controller simulation model.

As shown in Figure 1, the input of the logic controller is connected to the output U^*_i of the speed regulator and the feedback signal U_i of the current, respectively. The rectifier switching signals output by the controller are U_{blf} and U_{blr}. They control whether to output a phase shift trigger pulse through the trigger module. The requirement of the block end of the trigger module is: when the signal output by the logic controller is "0", the trigger allows the output pulse; if the signal output by the logic controller is "1", the trigger has no pulse output.

5 Simulation and debugging

Since we must consider the data type of the delay module during the simulation, a data type conversion module has been added, as shown in Figure 2.

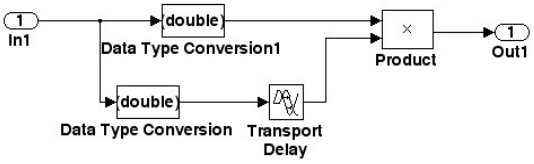

Figure 2. Delay module structure.

In the module shown in Figure 2, the turn-off delay time is set to about 3 milliseconds, and the open delay time is set to about 7 milliseconds.

When the given signal is working, the Ublf output can be seen as 0 in the oscilloscope SCOPE3 connected to the DLC output. Therefore, this signal is given to the positive group. The simulation result is shown in Figure 3.

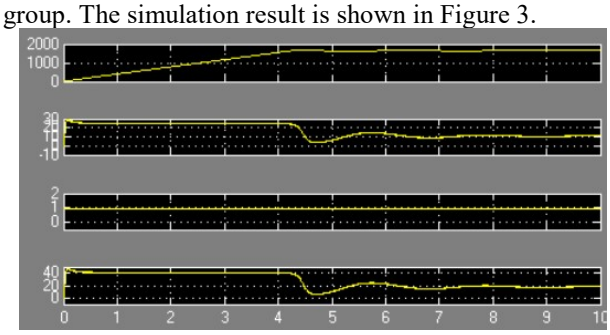

Figure 3. DLC control forward rotation waveform.

When the negative reference signal is working, we can see that the Ublr output is 0 in the oscilloscope SCOPE3 connected to the DLC output, so this signal is given to the inverse group. The simulation results are shown in Figure 4.

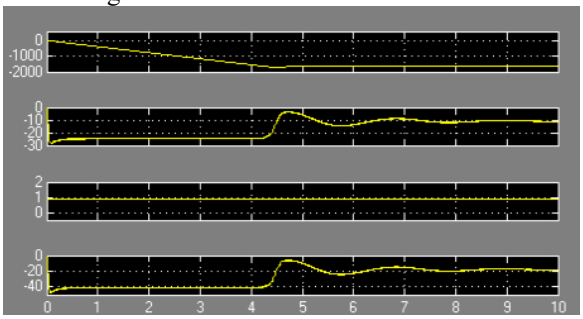

Figure 4. DLC control inverted waveform.

6 Summary

When the transition process of the process system does not require high smoothness, from the perspective of production reliability, a loop-free reversible system with neither a DC average circulation nor instantaneous pulsation is used. In production practice, the non-circulating DC speed adjusting system is often used. And the DLC is the core element of the non-circulating DC speed adjusting system. A simulation model of the logic controller DLC in the reversible DC speed control system was established. The parameters of the DLC were set. The reversible system obtained forward and reverse waveforms was obtained. And the simulation results surface: the method is correct and feasible.

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