

Integrated technologies and the problem of creation of large-area silicone carbide devices for high-power converters

Tatiana Ilicheva¹, and Eugeny Panyutin^{2*}

¹Admiral Makarov State University of Maritime and Island Shipping, 198035, St-Petersburg, Russia

²Ioffe Physical Technical Institute, 194021, St-Petersburg, Russia

Abstract. We consider limitations typical for semiconductor devices of up-to-date converter equipment based on silicon and silicone technologies. The reasons for processing complexities in creating the hardware components of heavy-current devices based on wide-band-gap semiconductors are analyzed. Possible approach to production of large area SiC-diodes and thyristors is formulated, which at post-processing stage allows performing modification of their voltage-current characteristics (VCC) and increasing in its non-linearity coefficient. Based on the concept of integrated power devices containing mesa-elements with VCC with random parameters, the possibility of sequential automated exclusion of those single “non-standard” micro-devices to adversely impact on general voltage-current characteristics of an array is considered. Algorithm is briefly described, and computer modelling of transformation of the reverse branch of integrated VCC occurring in the course of such modification is provided, which made it possible to establish relationship between the typical probability distributions of impurity (including in the presence of dislocations) and certain features of final VCC.

1 Introduction

Thyristor converters (power controlled rectifiers, rectifying inverting aggregates, pulse converters) capable of providing the smooth adjustment of current and voltage, changing frequency and converting of time characteristics of pulses represent an integral component of modern electromotive power plants to date. According to its functional purpose (dc/mac conversion, pulse-width or frequency-width modulation, etc.), such converters can provide optimal control of various types of motors, in particular DC motors, commutatorless multi-phase or asynchronous motors. Key elements in such converters are heavy-current diodes and thyristors. As known, operation of these devices is based on the processes in *pn*-junctions, and despite technological advances in development of devices based on other appropriate materials, for example, SiC, main production volume of such industrial valves

* Corresponding author: eugeny.panyutin@mail.ioffe.ru

are still concentrated on silicon and are being implemented in the framework of traditional silicon technologies.

In many instances, such situation is due to the fact that a number of important electrical parameters and characteristics of thyristors have arrived to dramatic values by now. For example, blocking voltages range is 8000V and even more, and average current of a single one-chip device reaches 3000A (with near 100 mm plate diameter).

Nevertheless, there are a number of important characteristics relating to reliability and durability of Si-devices or long-term stability of their parameters, a need for improvement of which has arisen a long time ago. Particularly, operational life of high-power thyristors and even diodes is still far behind the similar parameter not only for the entire electromotive as a whole, but also behind the resource of other accompanying elements something like transformers and resistors. Additionally, fault tolerance of conventional thyristors, which is in many instances definable by probability of developing the spontaneous regenerative processes accompanied by current localization and uncontrolled increase in local heat evolution, does not always satisfy the desired requirements. Further, even without considering possibility of local overheating, maximum allowable operating temperature of silicon *pn*-junctions should not exceed 125 °C, which imposes unambiguous restrictions to allowable average current density.

These days, it seems quite certain that advancement of semiconductor technologies towards further development of wide-band gap materials and in the context of final problems as well, and taking into account specifics of obtaining heavy-current devices, would contribute to at least partial solution of this set of problems [1-3]. Indeed, since such important material features as mechanical strength, parameters over time stability and heat stability for materials from classes A^{III}B^V and A^{IV}B^{IV} at least correlate to a certain extent with the values of width of their band gap E_g , then pursuant to increasing the limit temperature of *pn*-junction operation, they could form the following series: GaAs: $T_{\max}=250$ °C; GaP: $T_{\max}=400$ °C; GaN: $T_{\max}=500$ °C; SiC-4H: $T_{\max}=600$ °C. Since fault tolerance and operational life of a device is directly related to heat and radiation stability of its material, polytypic silicone carbide 4H (SiC-4H, $E_g=3.35\text{eV}$) is considered to be the most promising semiconductor material in the context of concern and satisfying a number of additional necessary conditions.

2 Problem and feasible approach to its solution

However, fundamental challenge is that opposed to silicon and traditional silicon technologies, creation of even single-junction devices — diodes — but with ~ 100A typical operating currents and in one-chip version based on SiC involves considerable processing complexities. It is well known that in case of wide-band gap materials, attempts to increase structure's working area (up to ~ 1cm² or more) necessary for required currents to flow in a single device result in a sharp decrease in the process yield of *pn*-junctions with a defined area of output parameters. This applies particularly to the values of maximum blocking voltage or allowable direct current; moreover, probability of “short circuit” to exist in device's operational field is noticeably increasing. For example, nominal current values for one-chip SiC diodes do not exceed 20A [4-5] to date.

Such situation is indicative of overall level of the entire processing chain, and it should be appreciated that epitaxial technologies for generation of silicon carbide multilayer *pn*-structures differ in many respects from diffusive silicon ones. At the same time, numerous uncontrolled factors accompanying each of the processing stages — from substrate material procurement to post-epitaxial operations — cause spatial microinhomogeneity of interface regions to appear near *pn*-junctions on the entire area of the device structure. The main source for appearance of such microinhomogeneity is doping impurities concentration

fluctuations during the high-temperature phase of epitaxy, which relates without limitation to specificity of certain diffusion mechanism, and with local migration processes in the area of grid distortion near dislocations, and with generation-recombination of intrinsic point defects. As a consequence, a complex concentration relief arises that forms locally curved surface of *pn*-junction with significant fluctuations in its local effective width. The whole of the above circumstances, taking into account non-linear character of voltage-current characteristics of junctions, is a reason for significant (much larger than in case of silicon *pn*-junctions) statistical variability of VCC in the series of devices [6].

Despite significant efforts aimed at increasing in homogeneity of the parameters of device structures and reduction of such dispersion, “head on” solution of this problem for SiC, i.e. by reducing the concentration of dislocations of initial substrate single-crystal chips or improvement of epitaxial methods, progresses rather slowly; so that main finishing process technique is still a method of rejection of small area single-chip discrete devices and their subsequent assembly into multi-crystal heavy-current modules [7]. Although such approach is justified in certain special situations (high temperatures, elevated background radiation), in general, it does not solve reliability and durability problem due to the presence of external interconnections.

Another feasible approach to solution of the problem, which, as expected, is supposed to contribute to creation of a new generation of more high-power devices, including those based on SiC, reaches out to microtechnology means and assumes a full use of photolithography possibilities.

It is assumed that at the first stage a large array of microdevices (microdiodes) should be formed on the basis of a large area *pn*-structure (which in the simplest case contains one *pn*-junction) (for example, in the form of mesa-structure). It should be noted that methods of microelectronics in silicon technology of some heavy-current devices have been used for a long time and with success, however, in this case their use is oriented toward solving completely different problems [8-12].

Main concept of the proposed method is creation by means of microlithography of certain conditions for further correction of some important VCC parameters of a final integrated device, namely, such conditions that could provide the possibility of automated elimination of defective areas such as “short circuits” or local areas with lower than normal threshold of collision ionization onset at the “post-processing” stage.

From a technology viewpoint, the method is close to realization of an idea of obtaining programmable logic matrices with fusing jumpers (Antifuse technology for silicon), i.e. creation of a predefined circuit configuration of transistors by feeding the fusing pulses to corresponding pairs of cross-buses, which provides appearance of bursts in the required places, see [13-14] for example. Nevertheless, the method differs fundamentally from the latter both in the tasks being solved and peculiarities of its implementation, and, as will be further shown, a controlled change in the shape and VCC features may occur as a result of action to integrated device of a long series of pulses produced in the final phase of post-epitaxial stage.

Such a path, although it increases load on the post-epitaxial technology phase, significantly improves output characteristics of devices. In the capacity of the first stage of method implementation, mesa-relief should be created on the entire area of the device's operating area, which also includes a non-rectifying contact. By means of several additional operations — creation of an insulating layer, application of additional layer of metal and using appropriate lithography, a structure can be formed, which topology corresponds to the system of parallel-connected local circuits of the “mesa-diode and resistive junction series-connected with it” form united by a common non-rectifying contact. The final operation is anisotropic etching-out of under-resistor pits, which allows for representing the jumpers as

airy bridges, where the width of each bridge must be small enough (2-10 mcm) and allow for its destruction by a current pulse when it exceeds a certain critical value i_{cr} .

In this case, post-processing pulse action (with the reverse junctions bias) will lead to the following process: as voltage increases in a step-by-step manner in accordance with increase in the pulse number, a corresponding increase in current controlled by diodes and, therefore, individually distributed in local circuits will lead to sublimation of some of the jumpers at certain steps. Therefore, the subsequent bursts in these circuits will ensure exclusion of such “non-standard” diodes from further participation in group activities of the entire array. Since such critical currents (if equipotentiality at common contact condition is met) will be achieved first of all for diodes characterized by low breakdown voltages or high leakage currents, these diodes will consistently steer away leading to a stepwise transformation of the reverse branch of total VCC. Thus, in the course of such impulse action, an algorithm will be implemented for automated rejection of unacceptable mesa-diodes regardless of their spatial arrangement. It is apparent that for a timely process shutdown, VCC change control must be carried out in real time. Considering that maximum sizes of mesa-element together with resistor may be sufficiently small (20×20 mcm or even less), their total number in a multi-device can reach $\sim 10^6$ or more; in this case, conventional linear methods of testing, sorting and subsequent robotic assembly seem to be ineffective.

3 Computer modelling and results

For illustration of the foregoing, computer modelling of transformation of the reverse branch of multi-device's integrated VCC was carried out in the course of gradual elimination of “weak points” for the cases of different probability distributions of N_D , N_A doping impurities concentration and parameters of local devices characteristics. It is assumed that at this modelling stage all fluctuating parameters are globally homogeneous, i.e. their statistical averages are independent on location on the chip and, in addition, spatially uncorrelated, and correspondence of real geometry of the device is limited only by correspondence of the characteristic dimensions. Such multi-device can be represented as a set of K parallel-connected mesa-diodes, where each of which, according to a specific set of local concentrations of N_A and N_D -layers, will have its own VCC. The required number of M fusing pulses in a series must correspond to expected number of defective diodes and in particularly adverse cases may constitute $M \sim K$.

As a first approximation, for each of the local diodes, a simple three-parameter approximation of the reverse branch of its VCC definable by voltage of origin of avalanche breakdown U^{br} , as well as parameters of conductivities g^{pre} and g^{post} of linearly increasing currents, respectively, before and after breakdown, may be used. It is also assumed that for some of reverse-biased junctions their conductivities values can also reflect the presence of notable contribution of the tunnel current component. Then, characteristic of each of the local diodes can be represented by piecewise linear function

$$i_{m,k}(U_m) = g_k^{pre} \cdot U_m \quad 0 < U_m < U_k^{br} \quad (1)$$

$$i_{m,k}(U_m) = g_k^{post} (U_m - U_k^{br}) \quad U_m > U_k^{br} \quad (2)$$

Here, n is a local diode number in the array, m is a pulse number in the series. The presence of experimentally observed dispersion can most adequately be interpreted from the perspective of stochastic functions theory; in this case, $i_k(U)$ can be construed as the k -th realization of the discrete stochastic function $\{i_m(U_m)\}$, which depends on random parameters $\{g^{pre}\}$, $\{g^{post}\}$, $\{U^{br}\}$, provided that $i_{k,m}(U_m)$ is a value of this implementation for

the m -th pulse. A typical type of VCC family of local mesa-diodes formed on the basis of a pn -structure with randomly inhomogeneous doping is shown on Fig. 1.

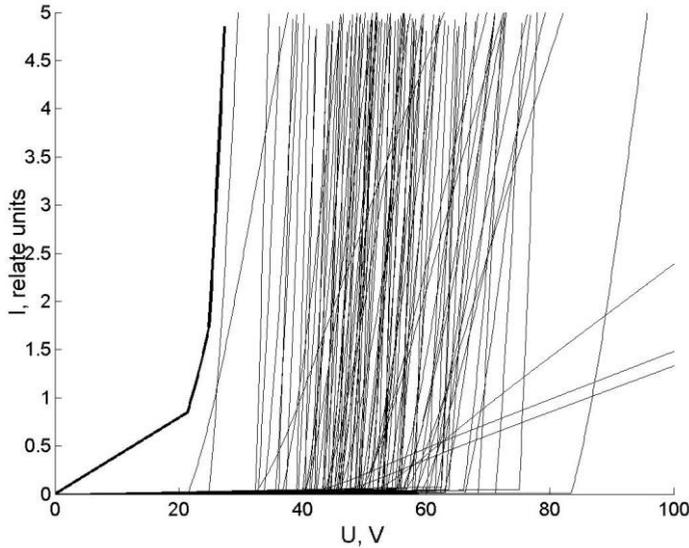


Fig. 1. Reverse branches of VCC (including avalanche breakdown regions) of the local diodes constituting the matrix. Heavy line to the left is an integrated diode VCC.

Since these random parameters, each of which characterizes the reverse branch in its own way, are very sensitive to local specificity of concentration profiles of impurities near the junction and, accordingly, electric field profiles, the choice of distribution laws corresponding thereto should be based either on experimental data or general theoretical considerations.

At its simplest (in the absence of large-scale distortions of a grid of dislocation type), spatial fluctuations in doping concentrations may be characterized by $\{N_d\}$ function with Gaussian distribution. Taking a globally averaged value of N_{do} (for example, 10^{18}cm^{-3}) as mathematical expectation, dispersion of this distribution, depending on the ratio of spatial scale of mesa-diode and the Debye screening distance, can be estimated as $(0.01 \div 0.2) \cdot N_{do}$. However, for materials under consideration, situation is more realistic when dislocations in notable quantities are not only present, but are also, in many cases — both for donors and acceptors — effective drains, thereby creating favourable conditions for appearing the local regions with their higher than normal ($>10^{19}\text{cm}^{-3}$) concentration. In this case, probability distribution $\{N_d\}$ takes the form of “double-humped” distribution. Assuming, further, for simplicity of $N_A = N_D = \{N_d\}$, and using known relations for voltage of avalanche breakdown and tunnelling current of pn -junction (see, for example, [15]),

$$U_{br} \approx 60 \cdot (E_g / 1.1)^{3/2} \cdot (N_d / 10^{16})^{-3/4} \quad (3)$$

$$i_t = (((2m^*)^{1/2} \cdot e^2) / (4\pi \cdot h^2 \cdot E_g^{1/2})) \cdot E_{pn} \cdot U_{pn} \cdot \exp(-(4(2m^*)^{1/2} \cdot E_g^{3/2}) / (3e \cdot E_{pn} \cdot h)) \quad (4)$$

and also taking into account that both the field in pn -junction E_{pn} and voltage U_{pn} are functions of N_d , the entire set of random breakdown parameters $\{U_{br}\}$, conductivity $\{g^{pre}\}$ and $\{g^{post}\}$ may be obtained.

The next phase of calculations consisted in obtaining the whole set of K functions, each of which represented one of $i_k(U)$ implementations for all values of U_m and corresponded to

a certain local diode. Next, we calculated the “global” characteristic; taking into account diodes paralleling, it was $I(U)$ superposition of these implementations. And only then actual pulse action process itself was being modelled, when K -array was sequentially scanned, and at each step m a search was made for functions i_k , for which at least one of $i_{k,m}$ values would satisfy $i_{k,m} > i_{cri}$ condition; in case of its performance, corresponding functions (i.e. which turned out to be a “weak link”) were removed from the array. Finally, at each step m , VCC superpositions of such “truncated” $I_m(U_m)$ arrays were calculated. Since all functions are assumed to be monotonous (absence of N-shaped and S-shaped regions), transformation of VCC reverse branch may be characterized by introducing any suitable functional, for example, $I_{max, m} = \max(I_m)$.

According to above scheme, the matrices were studied (for definiteness, $E_g = 3.3eV$), which included 25×25 mesa-diodes with 0.4 mm diameter for different probability distributions of N_d concentration near the junction; VCC of integrated device $I_{int}(U)$ was carried out within $0 \div 80V$ range; critical current $I_{cri} = 10^{-5}A$ value was used. Figure 2 shows a family of curves (for four different values of N_{do} math. expectation), which demonstrated decrease in $I_{max, m}$ logarithm (all I_{max} values correspond to $U_{max} = 80V$ voltage) as N_{dis} (disconnect) number of the excluded diodes increases.

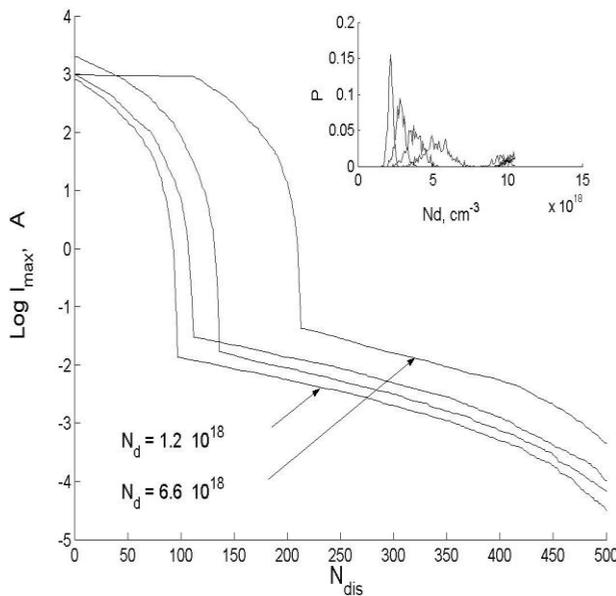


Fig. 2. Curves reflecting dependence of integrated device reverse current logarithm (for $U_{rev} = 80V$) on the number of “disconnected” mesa-diodes for 4 mean values ($N_{do} = 1.2 \cdot 10^{18} \text{ cm}^{-3}$, $N_{do} = 3.0 \cdot 10^{18} \text{ cm}^{-3}$, $N_{do} = 4.8 \cdot 10^{18} \text{ cm}^{-3}$, $N_{do} = 6.6 \cdot 10^{18} \text{ cm}^{-3}$). At the upper right is a family of corresponding probability distributions of mesa-diodes array $\{N_d\}$ concentration.

Practically speaking, it is also interesting to estimate the average number of diodes N_{int} , which have passed the pulse screening procedure, including, in case of restrictions imposed to $I_{max, m}$, which, for example, did not allow for exceeding a certain level I_{lev} (in this case, I_{lev} values were $2.5 \cdot 10^{-4}A$, $7.3 \cdot 10^{-5}A$, and $6.3 \cdot 10^{-6}A$, respectively). The curves corresponding to a change in this average “matrix occupation number” depending on N_{do} are shown on Fig.3. All calculations were performed in MATLAB environment.

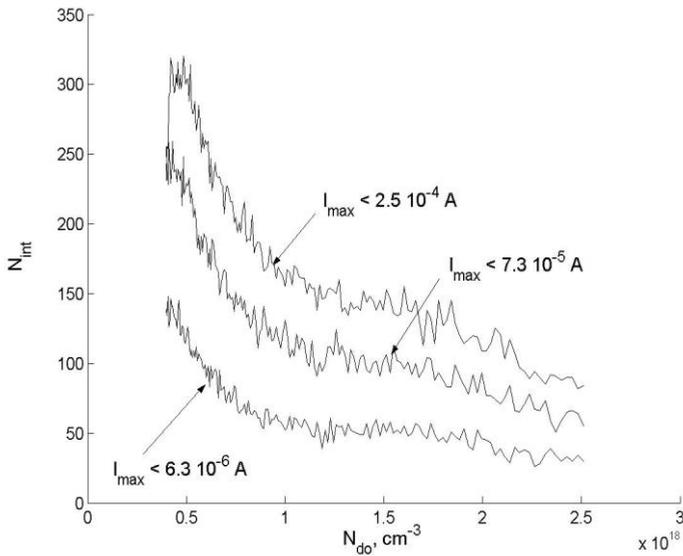


Fig. 3. Dependence of the average number of mesa-diodes N_{int} having successfully passed the screening procedure on the average concentration of N_{do} . Results for different levels of maximum integrated current $I_{max,m}$ limitation are represented.

4 Conclusions

Thus, procedure for automatic elimination of the defective areas of pn -structure and its accompanying auto-adjustment of VCC will contribute for more efficient use of its area. It is assumed that the said approach will not only facilitate the production of more high-power GaN- and SiC-diodes and thyristors, but also provide the possibility of implementing more stringent tolerances for parameters in the series of integrated devices intended for operation as a part of a single and a converter module, which, as is known, leads to additional increase in overall fault tolerance of the converter

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