Design of low-power 2FSK demodulation circuit

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Abstract. Aiming at the complex structure and high power consumption of the existing 2FSK demodulation circuit, this paper designs a simple structure and low power 2FSK demodulation circuit. A CMOS transistor matrix circuit is used to demodulate the 2FSK signals of 1200HZ and 2200HZ. The function model is established by using Matlab, and the number of sampling points is determined according to the simulation results and design requirements, and then the size of CMOS transistor matrix circuit is determined. The circuit uses Cadence software for functional verification, and HSPICE software is used for power consumption analysis. The simulation results meet the design requirements of low power consumption and achieve the desired demodulation effect.

1 Introduction

The HART protocol is a fieldbus protocol widely used in instrumentation, this protocol is a two-way protocol proposed by the US company Rosement in 1985, and is the abbreviation of the remote addressable data channel transmitter protocol [1]. The modulation and demodulation technology used by the physical layer of the HART protocol is FSK (Frequency Shift Keying) technology. A digital signal with an amplitude of 0.5 mA and an average value of 0 is superimposed on an analog signal with an amplitude of 4 to 20 mA, representing the "1" and "0" of the digital signal with 1200 Hz and 2200 Hz AC signals respectively, which realizes the transmission of digital signals on the analog channel without mutual interference [2] .

Since the HART protocol is widely used in low-power applications, the FSK demodulation circuit of the core circuit of the HART protocol has low power consumption requirements. At present, methods for implementing FSK demodulation include coherent demodulation method, non-coherent demodulation method, frequency discrimination method, zero-crossing detection method, and difference method, although these methods can realize demodulation of FSK signals, however, these methods generally require the use of high-performance filter circuit, differential circuit, integration circuit, rectifier circuit, detection circuit and other complex circuits [6], and the use of these complex circuits also makes the overall circuit power consumption extremely high, it is difficult to meet the practical needs of low power consumption. This paper designs a low-power 2FSK demodulation circuit and performs functional simulation and power analysis. The simulation test results show that the designed circuit can realize 2FSK demodulation function, and the power consumption reaches the practical standard.

2 Design of CMOS transistor array circuit

2.1 Demodulation circuit overall functional block diagram

The overall block diagram of the 2FSK demodulation circuit is shown in Figure 1, First, the 2FSK signal is converted into a digital signal with only high and low levels through a voltage comparator. Then, the CMOS transistor array circuit performs sampling of the digital signal and latching the sampling result under the control of the digital circuit. Finally, the digital control circuit outputs the demodulation results of the CMOS transistor array in serial data.

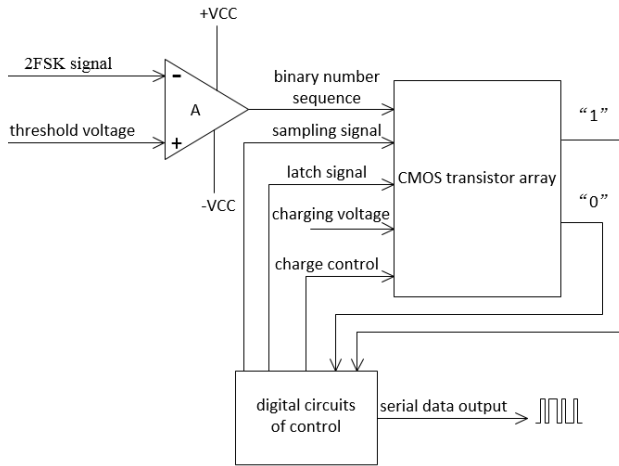
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Figure 1. Demodulation circuit overall functional block diagram

2.2 The working principle of CMOS transistor array circuit

The structure of the CMOS transistor array circuit is shown in Figure 2. The NMOS transistor is used as a switch. 1 represents a high level and 0 represents a low level. When the gate of the NMOS transistor is connected to a high level, the switch is in an on state, and the source voltage of the NMOS transistor is approximately equal to the drain voltage. When the gate of the NMOS transistor is connected to a low level, the switch is in an off state, and the source voltage of the NMOS transistor is approximately equal to 0, each switch correspondingly detects one bit binary number, and multiple switches cascade to realize detection of binary numbers sequence.
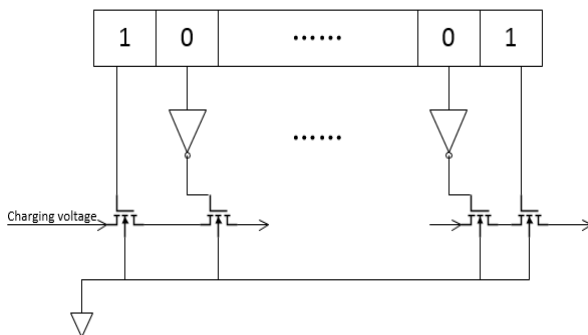

Figure 2. CMOS transistor array circuit structure diagram.

2.3 Establish matlab simulation modele

The 2FSK signal consists of a sinusoidal signal with a frequency of 1200HZ and 2200HZ, and is sampled using a signal with a frequency of F_S, there exists the following equation.

$$F_S = N \times 1200 \ (N \text{ is integer}) \tag{1}$$

The size of N is adjusted constantly until one signal cycle time of the 1200HZ signal, the binary number

sequence obtained by sampling the 1200HZ signal is quite different from the binary number sequence obtained by sampling the 2200HZ signal, and F_S is the frequency of the sampled signal, and N is the number of sampling points in one signal period.

Since the 2FSK signal will have noise interference during channel transmission, the noise makes the output of the comparator near the threshold voltage uncertain, which leads to the uncertainty of the obtained binary sequence, therefore, the influence of noise must be considered when determining the number of sampling points. In order to be able to demodulate correctly, the data sampled near the comparator threshold voltage is discarded, and the discarded data points are replaced by "X".

The bit error rate of the 2FSK signal exists the following equation.

$$SNR = 20lg^{\ (VS/VN)} \tag{2}$$

SNR is the signal-to-noise ratio and *VS* is the effective value of the 2FSK signal amplitude and *VN* is the effective value of the noise amplitude.

The angle *A* of the interval between every two sampling points can be obtained from the number of sampling points, there exists the following equation.

$$A = \frac{2\pi}{N-1} \tag{3}$$

The number *SN* of sampling data deviations caused by the noise near the comparator threshold voltage can be obtained from equations (2) and (3), there exists the following equation.

$$SN = \frac{\arcsin\left(\frac{VS}{10^{\frac{SNR}{20}}}\right)}{\frac{2\pi}{N-1}} \tag{4}$$

In the 2FSK signal, the frequency of the 1200HZ signal and the 2200HZ signal are converted into a binary number sequence by the voltage comparator, and the adjacent two high and low level flip point positions are different by $\pi/2$, from this, obtain the number of data points *FN* that can be sampled with F_S as the sampling frequency $\pi/2$ period, there exists the following equation.

$$FN = \frac{\pi/2}{A} \tag{5}$$

In order to realize the demodulation function, the number of sampling data deviations caused by noise should be less than *FN*, and the effective value of the noise amplitude should be converted to an angle of less than $\pi/2$, there exists the following equation.

$$\begin{cases} FN - SN \geq 1 \\ arcsin(VN) \leq \pi/2 \end{cases} \tag{6}$$

The relationship between the number of sampling points combining equations (2), (3), (4), (5), and (6), there exists the following equation.

$$\begin{cases} N \geq \dfrac{4arcsin(\dfrac{VS}{10^{\frac{SNR}{20}}})}{\dfrac{2\pi}{N-1}} + 5 \\ SNR \geq 20lg^{VS} \end{cases} \quad (7)$$

The condition of Matlab simulation model designed in this paper is *VS*=5V, the effective value of noise amplitude is 0.5V, and the *SNR* is 20dB. According to formula (7), *N*≥32, *SN*=1, in order to minimize the circuit scale, take *N*=32, Figure 3 and Figure 4 show the binary sequence of the 1200HZ and 2200HZ signals obtained by the model under ideal conditions and noise conditions.
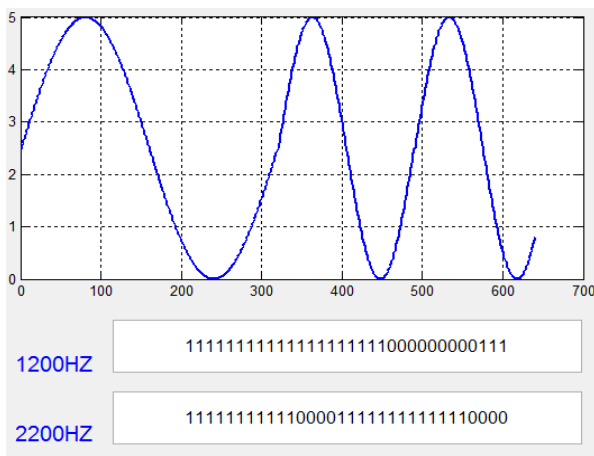

| 1200HZ | 1111111111111111111000000000111 |
| 2200HZ | 1111111111100001111111111110000 |

Figure 3. Simulation results under ideal conditions

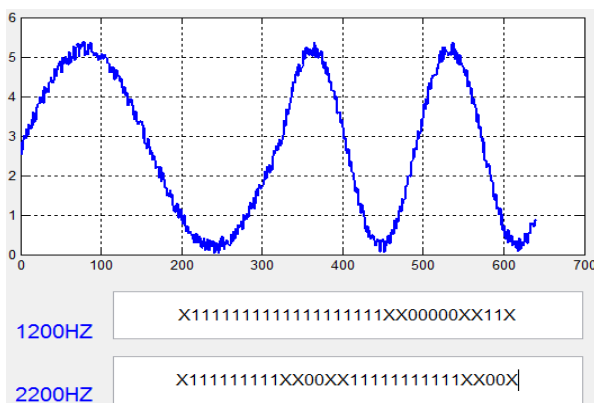| 1200HZ | X11111111111111111111XX00000XX11X |
| 2200HZ | X111111111XX00XX11111111111XX00X |

Figure 4. Simulation results with noise

2.4 Low power design

When a sequence of binary numbers causes all the switches in a row of the CMOS transistor array circuit to be in an on state, the charging voltage charges the parasitic capacitance of the CMOS transistor, and when all the parasitic capacitances of the row are fully charged, the output is high level. When the capacitance of the capacitor is fixed, the charging time

N and the error rate *SNR* can be obtained by of the capacitor is inversely proportional to the charging voltage, this requires the charging voltage to be high enough to fill the capacitor within one clock cycle of the sampled signal, and the power consumption of the circuit is proportional to the square of the voltage[3-4], this will undoubtedly increase the power consumption of the circuit and does not meet the design requirements. As shown in Figure 5, a latch is added between the shift register and the CMOS transistor array, Figure 6 is a waveform of the latch signal and the charge control signal, when the number of samples reaches 32 times, store the sequence of binary numbers in the shift register in the latch, and the charging voltage can slowly charge the capacitor in multiple clock cycles, which can greatly reduce the voltage value of the charging voltage, moreover, after the latch is added, only one parasitic capacitance is charged and discharged in each signal period, therefore, the charging and discharging frequency of the parasitic capacitor is lowered, so that the power consumption of the circuit is greatly reduced.
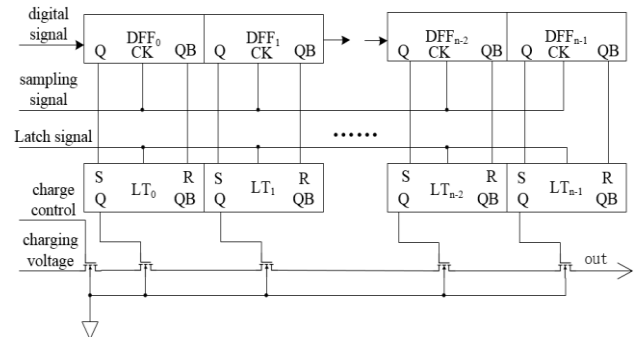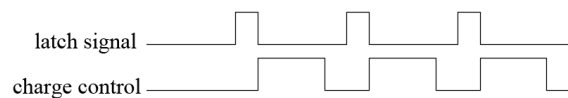

Figure 5. Low power design

Figure 6. Latch signal and charge control signal

3 Functional simulation and power analysis

3.1 Bit error rate analysis

The simulation circuit is built under Cadence for functional simulation [5], the function simulation results are shown in Figure 7, it can be seen from the simulation results that the 2FSK demodulation circuit can realize the basic demodulation function. After noise is superimposed on the 2FSK signal and the signal-to-noise ratio is scaled, inputting the circuit demodulate signal.The results of the demodulation are compared by error, and the relationship between different signal-to-noise ratios and circuit error rate is shown in Figure 8. The minimum signal-to-noise

ratio that the 2FSK demodulation circuit designed in this paper can accept is $20lg^\land VS$. When the signal-to-noise ratio of the 2FSK modulated signal is less than $20lg^\land VS$, the bit error rate of the circuit will be very high or even

signal, so increasing the *VS* can improve the noise immunity of the circuit.
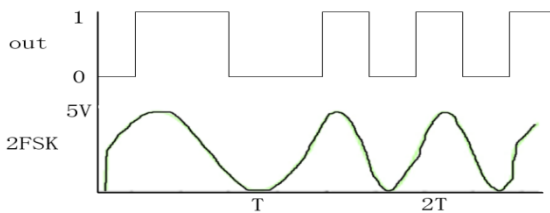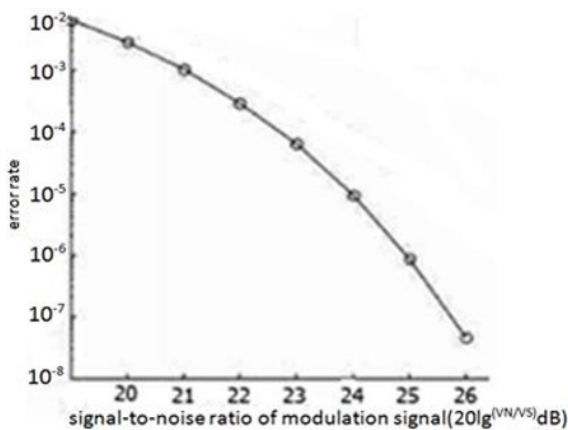

Figure 7. Functional simulation

Figure 8. Bit error rate curve

3.2 Power analysis

The power consumption of digital circuits is mainly reflected in dynamic power consumption, there exists the following equation.

$$p_{avg} = \frac{af C_{load} VDD^2}{2} \qquad (8)$$

a is the activity factor, indicating the number of times the capacitor is charged and discharged in one signal period, f is the operating frequency, *VDD* is the operating voltage and C_{load} is the parasitic capacitance. In this paper, f is equal to the sampling frequency.when the number of sampling points and the sequence of binary numbers are determined, *a* and f and C_{load} are all fixed values.

It can be concluded from (8) that reducing the dynamic power consumption of the circuit can be achieved by reducing the number of times the capacitor is charged and discharged in one signal period, reducing the sampling frequency of the circuit, reducing the parasitic capacitance of the circuit and lowering the operating voltage. Since the transistors used in the CMOS transistor array circuit designed in this paper are only used as switches, the minimum size transistor can be used to reduce the parasitic capacitance. Reducing the operating

not working properly. It can be seen that the signal-to-noise ratio that the circuit can withstand is proportional to the effective value *VS* of the amplitude of the 2FSK

voltage can reduce the power consumption of the quadratic, so reducing the operating voltage can greatly reduce the power consumption. The charging voltage of the array circuit is only 2V, and under the control of the charging control signal, only the parasitic capacitance in the circuit is charged and discharged once per signal period, operating voltage and operating frequency are greatly reduced compared to the same type of circuit, the method of reducing the operating voltage and lowering the operating frequency makes the demodulation circuit have lower power consumption.

4 Conclusions

Through simulation verification and power analysis, the feasibility and practicability of the circuit designed in this paper are proved, compared with the existing 2FSK demodulation technology, the power consumption is reduced under the guarantee of performance. Since the external conditions of the circuit operation are very different in specific applications, such as the difference in noise environment, this requires an appropriate increase or decrease in the size of the CMOS transistor array circuit depending on the specific application environment, balancing performance and power consumption.

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