Simulation Study of Overcurrent Turn-off Capability in 4500V IGBT

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Abstract. According to the requirement of IGBT's over-current turn-off capability, this paper analyzes the factors affecting the dynamic latch-up of IGBT chip during the over-current turn-off process, including the gate width of IGBT cell, the doping concentration of back P + collector and the dV_{ce}/dt when the IGBT is turned off. The simulation results show that the anti-dynamic latch-up capability of IGBT can be effectively improved by decreasing the gate width and back P + collector doping concentration. Through multi-cell parallel simulation, it is found that current concentration exists in the process of overcurrent trun-off, which leads to the further increase of the lattice temperature, and the overcurrent turn-off capability declines.

1 Introduction

In the new generation of high-power self-turned-off power electronic devices, IGBT (Insulated Gate Bipolar Transistor) devices have become the preferred devices in power electronic equipment. As an important application scenario of high-voltage IGBT devices, flexible-HVDC(High Voltage direct current) transmission technology has the advantages of independent control of active and reactive power, rapid regulation, and realization of large-scale power distribution, etc. It has broad prospects for development in large-scale renewable energy access, island power supply and new urban power grid construction[1]. As one of the core components of flexible-HVDC transmission, the high-voltage DC circuit breaker puts strict requirements on the IGBT device. The IGBT device needs to withstand 2~5ms duration, peak current equals to six times the rated current, and turn-off safely [2].

In this paper, the cell of 4500V IGBT chip is taken as the research object. Firstly, the factors affecting the over-current turn-off capability of IGBT chip are analyzed theoretically, including the width of gate, P-well doping concentration and back P+ doping concentration. Secondly, the cell structure model and device characteristics simulation model of IGBT are established in the Sentaurus-TCAD. The influence of each parameter is simulated and analyzed to guide the structure design and development of 4500V IGBT chip with high turn-off capability.

2 Analysis of turn-off capability of IGBT

2.1 Turn-off behavior of IGBT

In the case of flexible-HVDC transmission, the load of IGBT device is inductive load, and the schematic diagram of working circuit is shown in Fig.1, this is a typical clamped inductive application. L_s is the stray inductance of the circuit, L_{Load} is the load inductance, FRD (Fast Recovery Diode) is the freewheeling diode in the IGBT turn-off process, V_{ge} is the gate driving voltage of IGBT, generally a gate driving resistance R_g is connected between the driving power supply and IGBT gate, V_{cc} is the power supply voltage.

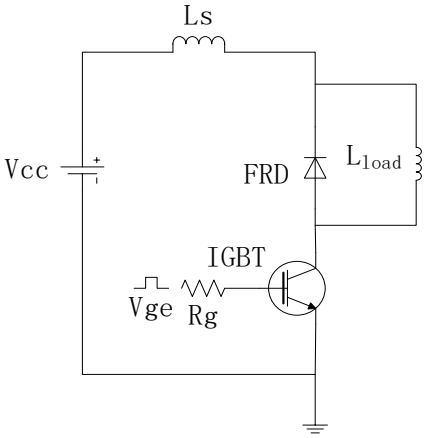

Figure 1. Schematic of working circuit

During clamped inductive turn-off transient, the stray capacitance in the IGBT play an important role in determining the turn-off behavior. The stray capacitance of IGBT consists of three parts, C_{ce} is the collector-emitter capacitance, C_{ge} is the gate-emitter capacitance, and C_{gc} is the gate-collector capacitance. C_{gc} consists of two parts, including oxide capacitor C_{ox} and PN junction depletion layer capacitance C_{dep}.

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The turn-off process of IGBT can be divided into four parts, as shown in Fig.2. All the four parts are as follows.

Part (1): When the turn-off signal is applied, the gate-emitter capacitance C_{ge} and Miller capacitance C_{gc} begin to discharge. The gate-emitter voltage V_{ge} falls down to a plateau and remains constant until the completion of the well-known Miller-effect[3]. In this part, since the FRD is still reverse biased, the load current I_L can not divert into the diode. The collector-emitter voltage V_{ce} and collector current I_c remain at their steady values. In the end of this part, the depletion layer slightly expanded, resulting in a slight increase in V_{ce} [4].

Part (2): When V_{ce} increases few volts, the part 2 starts. At this time, V_{ce} increases rapidly, the depletion region in the N-base begins to expand. This results in a great reduction of the depletion capacitance C_{dep}. Consequently, the Miller capacitance C_{gc} reduces to a much smaller value. After that, the gate drive only discharges the capacitance C_{ge}, the V_{ge} then decreases towards $V_{ge\ off}$. In this part, the load current cannot divert into the FRD. However, due to the large *dV/dt* at the anode side, the diode can still share a small part of load current. The IGBT current I_c then undertakes a slow decreasing.

Part (3): When V_{ce} reaches to V_{cc}, the part 3 starts. The V_{ge} falls below the threshold voltage V_{th}, the MOS electron current and the hole drift current associated with it are removed. This results in an initial rapid fall of I_c. Meanwhile, V_{ce} further increases by an amount equal to the voltage drop across the stray inductance L_S, which is well known as voltage overshoot of V_{ce}.

Part (4): When the V_{ce} falls back to V_{cc}, the part 4 starts. In this period, the V_{ce} approximately remains constant. The collector current I_c undertakes a slow decreasing due to the remaining excess carrier recombination in the undepleted n- base region and n+ buffer layer.

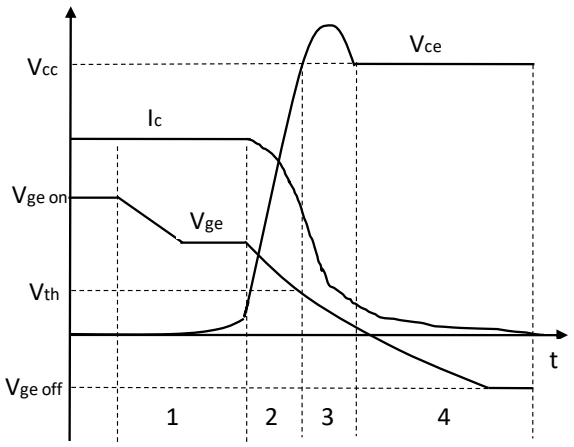

Figure 2. Typical waveforms of IGBT turn-off

2.2 Influence factors of IGBT overcurrent turn-off capability

During the over-current turn-off of IGBT chip, the current I_c remains at a higher level during the part 3, when the channel is closed and the current is all hole current. The hole concentration in the space charge region is given by equation (1).

$$p = \frac{J_c}{q v_{sat.p}} \tag{1}$$

The positive charge determined by the distribution of electric field inside the space charge is given by equation (2).

$$N^+ = N_D + p = N_D + \frac{J_c}{q v_{sat.p}} \tag{2}$$

From equation (2), it can be seen that the positive charge is greater than the intrinsic donor concentration during the turn-off process, which enhances the electric field of PN junction between P-well and n-base region, resulting in the decrease of breakdown voltage of the device, and this change is more obvious with the increase of the turn-off current.

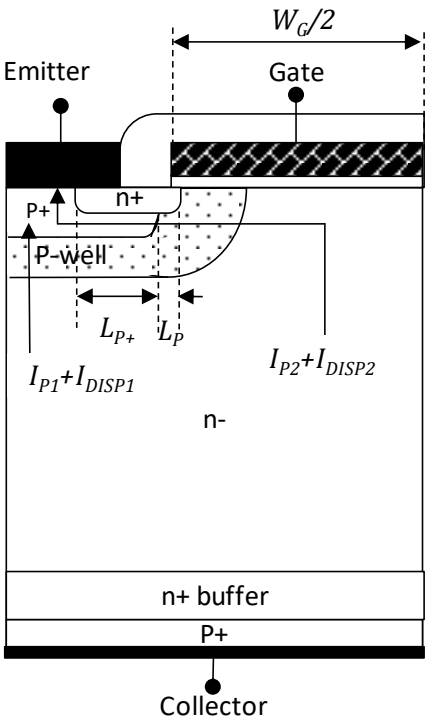

Figure 3. The half cell structure of IGBT

In this process, because all the current is hole current, the hole current density under the N+ source region is increased, and the latch-up condition is easy to trigger and the dynamic latch-up occurs. Since there is no electronic current component, the hole current injected by P+ collector becomes uniform in the device profile, so the criterion of dynamic latch-up can be determined as follows (3), and (4) ~ (7) gives the calculation formulas of each physical quantity. V_{bi} is the built-in potential of PN junction between N+ source region and p-well, which is about 0.7V at 125℃ and decreases gradually with the increase of temperature. The structure and parameters of IGBT are shown in Fig.3. I_{P2} is the hole current component injected into P+ collector region, I_{DISP2} is the displacement current component. $J_{C,ON}$ is the initial conduction current density. Z is the chip vertical to the section size. W_{ON} is the depletion layer width at initial conduction state, and it is used to calculate the

displacement current when the worst case is used for approximate analysis.[5]

$$(I_{P2} + I_{DISP2})R_B = V_{bi} \tag{3}$$

$$I_{P2} = \frac{J_{C,ON} W_G Z}{2} \tag{4}$$

$$I_{DISP2} = \frac{\alpha_{PNP} J_{DISP}}{1-\alpha_{pnp}} \frac{W_G Z}{2} \tag{5}$$

$$J_{DISP} = \frac{\varepsilon_S}{W_{ON}} \frac{dV_C}{dt} \tag{6}$$

$$R_B = R_{B1} + R_{B2} = \frac{\rho_{SP} L_P}{Z} + \frac{\rho_{SP+} L_{P+}}{Z} \tag{7}$$

Based on the above equations, the expression of current density limiting overcurrent is obtained (8).

$$J_{MAX} = \frac{2V_{bi}}{(\rho_{SP} L_P + \rho_{SP+} L_{P+}) W_G} - \frac{\alpha_{PNP} \varepsilon_S}{(1-\alpha_{PNP}) W_{ON}} \frac{dV_C}{dt} \tag{8}$$

It can be seen from the expression that the increase of dV_c/dt leads to the decrease of the turn-off current density during the turn-off process, and the change rate of collector voltage can be reduced by changing the gate drive resistance, but the turn-off loss can be increased. In terms of cell structure, enlarging gate width or reducing the emission efficiency of the back collector and the amplification ratio of the common base of the transistor can improve the current turn-off capability, but the effect of the reduction of the back collector injection efficiency on the $V_{ce(sat)}$ and short circuit capability should be considered. At the same time, the dynamic latch-up of IGBT can be restrained by reducing the resistance of P-well and P+, but it will bring adverse effects on the threshold voltage, so it needs to be carefully dealt with in the design.

In practice, IGBT chip is made up of large-scale cells in parallel. Due to the uneven distribution of current and the concentration of current during the turn-off process, some cells will withstand high current density during the turn-off process[6], resulting in high temperature locally, causing latch-up and chip burnout.

3 Simulation Results

The simulation analysis is carried out in the software of Sentaurus-TCAD. The mixed-mode of SDEVICE module is used to build the simulation circuit，each part of the circuit refers to the Fig.1. IGBT is generated by SPROCESS module, V_{cc}=3600V, L_s=6uH, L_{Load} = 1mH, $V_{ge\ on}$=+19V, $V_{ge\ off}$ = -15V, R_g=47ohm. The chip area is set to 1cm^2 and the rated current is about 60A, and the turn-off current value is set to 400A. We will compare the maximum lattice temperature to determine the risk of dynamic latch-up.

Fig.4 shows that the maximum lattice temperature varies with the doping concentration in the back P+ collector region. When the concentration increases, the hole concentration in the n-base region injected from the collector region increases, and the hole current density increases during the turn-off process, resulting in the increase of the lattice temperature and the risk of dynamic latch-up. Fig.5 shows the maximum lattice temperature varies with the change of gate width, when the gate width increases, the channel density decreases when the chip area and turn-off current are constant, and the hole current density in the P-well region increases during the turn-off process, which results in the increase of lattice temperature and the risk of dynamic latch-up.

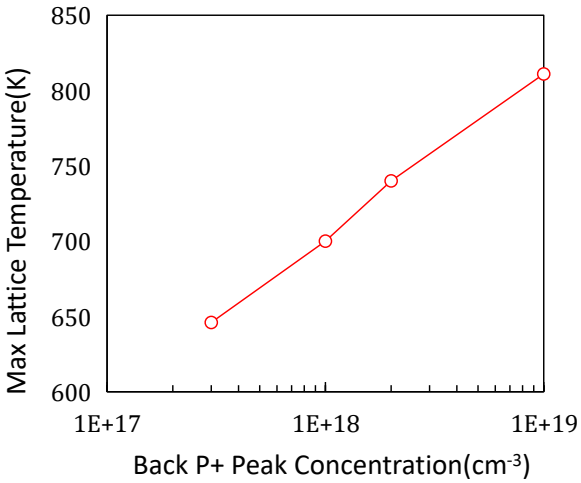

Figure 4. The maximum Lattice Temperature during overcurrent turn-off for the Back P+ concentration

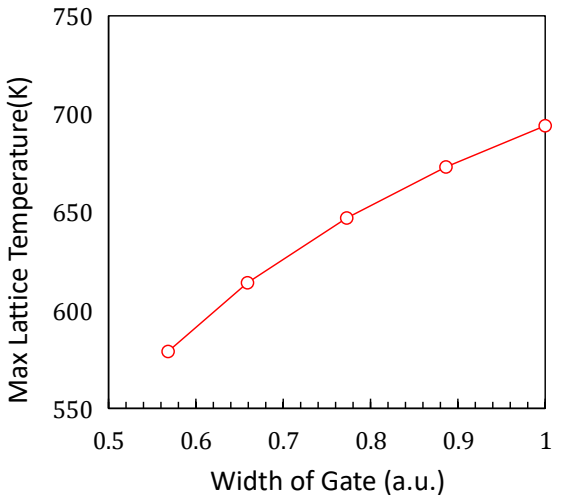

Figure 5. The maximum Lattice Temperature during overcurrent turn-off for the Width of Gate

In order to verify the actual situation of the chip, the multi-cell structure is simulated. The simulation results of different cell numbers are given in Fig.6. With the increase of the number of simulated cells, the maximum temperature of the lattice increases gradually. The main reason for this result is that the current distribution is not uniform during the turn-off process, and the current density of some cells is greatly increased. The current

density distribution of 16 cells at one time point during the turn-off process is given in Fig.7. It can be seen that the current density of 6 cells in the middle is significantly higher than others.

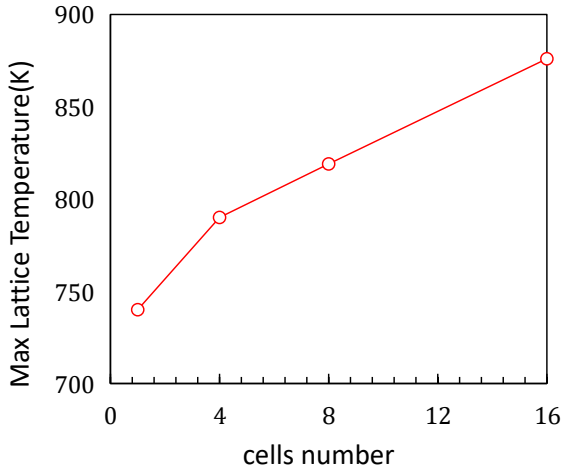

Figure 6. The maximum Lattice Temperature during overcurrent turn-off for the varies multi-cells

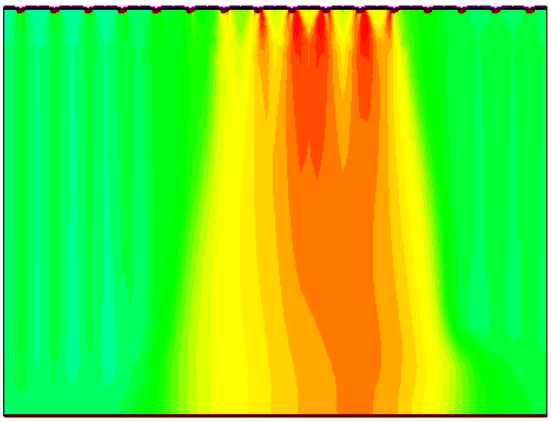

Figure 7. The current distribution during overcurent turn-off at sixteen cells array

4 Conclusion

Based on the theoretical analysis of the hole current in the IGBT turn-off process, the main cell structure parameters affecting the dynamic latch-up of the IGBT are P-well doping concentration, P+ doping concentration, gate width, back P+ collector doping concentration and so on.

The simulation results show that by reducing the gate width and back P+ collector doping concentration, the local lattice temperature rise of IGBT can be effectively reduced and the overcurrent turn-off capability of IGBT can be improved. From the simulation results of cell parallel connection, the current concentration during the cell parallel and the maximum lattice temperature are further increased. In the future, this phenomenon needs to be deeply simulated and analyzed.

Acknowledgement

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References

1. LIN Chang, ZHAI Xuebing, GAO Lu et al. Simulation Study of Control Strategy for Island Operation of Xiamen VSC-HVDC. Smart Grid, 2016,**4**(3):235-242.
2. WEN Jialiang, GE Jun, PAN Yan et al. Development and Expectation of Power Electronic Devices for DC Grid. POWER SYSTEM TECHNOLOGY, 2016,**40**(3):663-669.
3. Perpina X, Serviere J-F, Urresti-Ibanez J, CortesI,Jorda X, Hidalgo S, Rebollo J,Mermet-Guyennet M. Analysis of clamped inductive turn off failure in railway traction IGBT power modules under overload conditions. IEEE Trans Industrial Electron 2011;**58**(7):2706-2714.
4. Chokhawala RS, Catt J, Pelly BR. Gate drive considerations for IGBT modules.IEEE Trans Industry Appl 1995;**31**(3):603-611.
5. B.Jayant Baliga. *Fundamentals of Power Semiconductor Devices* . Spring Science+Business Media，LLC, 2008
6. Toechterle C, Pfirsch F, Sandow C, Wachutka G. Analysis of the latch-up process and current filamentation in high-voltage trench-IGBT cell arrays. Proc. SISPAD2013; 296-299.