A High-precision Current Sense Circuit with Trimming for DC-DC Converts

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Abstract. A high-precision current sense circuit with trimming is proposed to realize the over-current protection of the power management chip and improve its conversion efficiency. Based on solving the problem of voltage offset and current inrush caused by process deviation, this circuit can detect the value of the inductor current accurately. By designing the bandgap reference circuit and the reference voltage bias network, the required stable reference voltage and bias current can be obtained. The trimming bit selection circuit can realize the trimming function. This circuit is designed with TSMC 180nm 1P3M GEN2 process, and all circuits are verified by Cadence Spectre.

1 Introduction

Current detection can effectively improve the efficiency of the switching converter circuit and improve the stability of the power management system and the transient response speed([3], [5]). In addition, the inductor current reflects a large amount of information about the system, which can be used for current mode control, especially in multi-Phase conversion applications ([1]). The noise and offset of the traditional resistance detection system will eliminate the current information detected by the resistance, so high-precision current detection technology must be used([5]).

In order to obtain a stable reference voltage and a bias current, bandgap reference circuit and a reference voltage bias network is designed.

2 Design of high-precision current sense circuit

The high-accuracy current detection system is shown in Figure 1, the input is raised by a low-gain NPN transistor and there exist a base current I_b, the inductor current can be obtained as shown in the following formula.

$$I_L = \left(V_{csp} - V_{csn} \right) / R \qquad (1)$$

When Vcsn is greater than Vcsp, a negative voltage will occur. A negative voltage bias is required to drive the operation of the op amp and generate negative current.
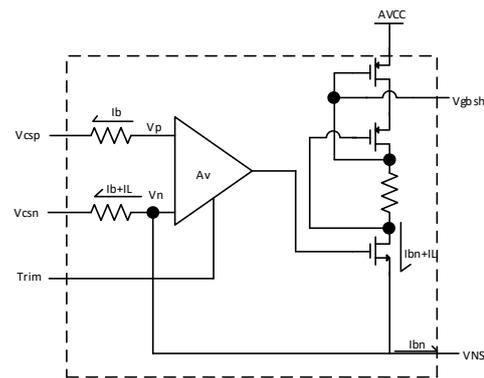

Figure 1. High-precision current detection system

2.1 High-precision current sense circuit

High-precision current sense circuit is shown in Figure 2, the circuit consists of the bias input stage, level shift circuit, trimming circuit, differential input casecode circuit, two-stage gain circuit and output stage circuit.

This circuit using NPN transistor as a differential input, we need to control the NPN transistor to work in the amplification area, in order to improve the op amp gain, reduce the random error (offset). It is necessary to use a level shift circuit to raise the output level, in order to make the current detection circuit work normally in the full output voltage range. The designed high-precision current detection circuit uses two levels of lift. The accuracy of the current mirror current is improved, by using a resistor self-bias cascode current mirror structure circuit .

In the self-bias circuit, the gate voltage of the common gate M10 is set by the resistor R3, which can reduce the power consumption and increase the power consumption. To ensure that all the tubes are in the saturation region,

the voltage drop IR_3 on the self-bias resistor needs to be defined. The drain voltage of the common-gate transistor M10 will be too low, and may exit the saturation region, when the self-biasing resistor R3 is too large. Through analysis, the selection of the resistor R3 is as follows.

$$\left[(V_{T10} - V_{T11})/I_{MIN}\right] \le R \le \left(V_{T10}/I_{MAX}\right) \qquad (2)$$

In addition, the circuit also includes trimming and negative current generating circuits for trimming the offset voltage and solving current inrush caused by process deviation by process variations.
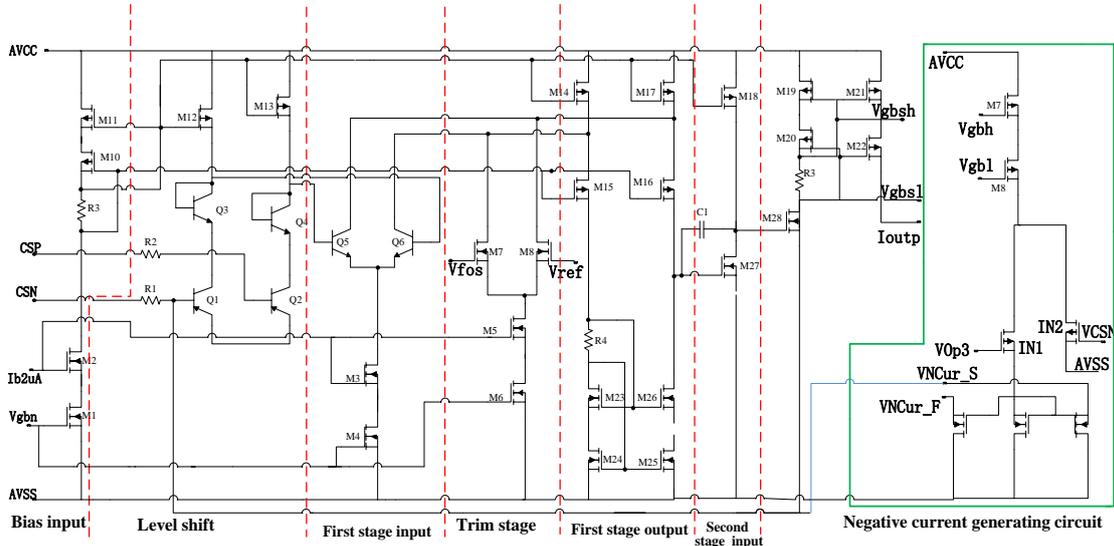

Figure 2. High-precision current detection circuit

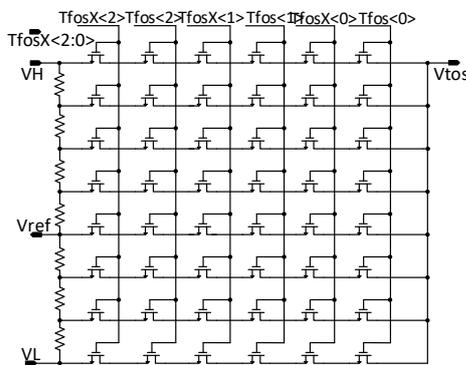## 2.2 Trimming selection bit circuit

Figure 3. Trimming bit selection circuit

As shown in Figure 3, the trimming selection bit circuit calculates the trim voltage value to be selected through resistor division. The top of the circuit is the trimming selection bit, and there are three trimmings. During trimming, the output voltage is measured at the same input voltage and compared with the ideal value. By changing Vfos, the output voltage approaches the ideal value. The trimming circuit modulates the circuit in the form of negative feedback.

2.3 Negative current generating circuit

The negative voltage bias circuit is shown in Figure 4. This circuit consists of a differential input and a bias current source. One of the input is connected to a fixed reference voltage VOp3, and the other end is connected to the VCSN.
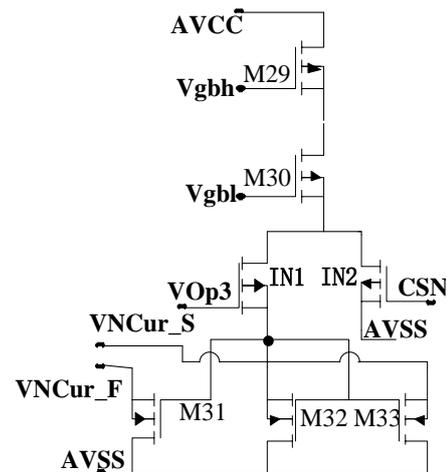

Figure 4. Trimming bit selection circuit

The current mirror provides current that flows into the reference voltage terminal, when the VCSN is higher than the reference voltage, the negative biasing module operates to provide a negative bias current for the current sensing module. Otherwise, the chip is in protected state and the negative biasing module does not work.

3 Design of bandgap voltage reference circuit

The bandgap reference voltage source circuir consists of four parts: BG, folded cascode feedback circuit, bias circuit and startup circuit, as shown in figure 4. The BG and op amp feedback circuits form the core circuit. Folded cascode op amps are used to increase the gain of the bandgap reference and increase the power supply rejection of the reference circuit. In order to improve the

anti-interference ability of the circuit, an output filter capacitor is added to the reference output.

The proportional coefficient k is shown in Equation [3], and this circuit can obtain a temperature-independent reference voltage.

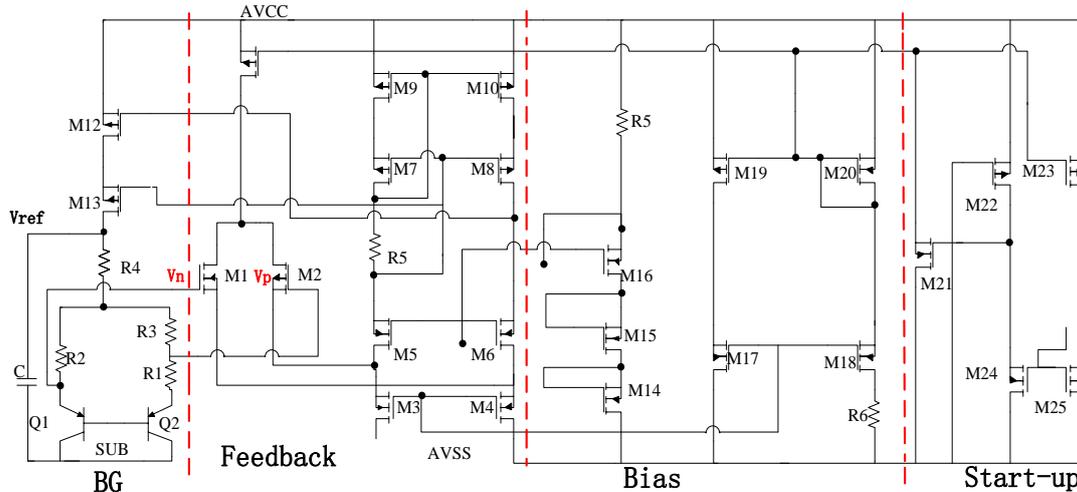$$K = \frac{R_2 + 2 \cdot R_4}{R_1} \tag{3}$$

Figure 5. Bandgap reference voltage reference circuit

4 Design of reference voltage and bias current network

The reference voltage circuit is shown in Figure 5, the reference voltage network is actually a buffer made up of an operational amplifier, making the differential input pairs equal in voltage. According to the voltage requirements of other module circuits, the resistance is selected and set. In order to reduce the mismatch of the system, the folded cascode structure is generally used.
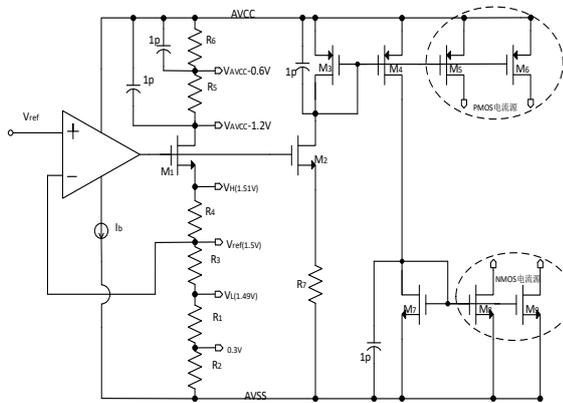
Figure 6. Reference voltage network

5 Simulation and analysis

5.1 Reference Power Circuits

The Bode diagram of the reference power supply circuit is shown in Figure 6. The phase margin is allowed to be around 40°, so the bandgap reference stability designed in this paper satisfies engineering applications.
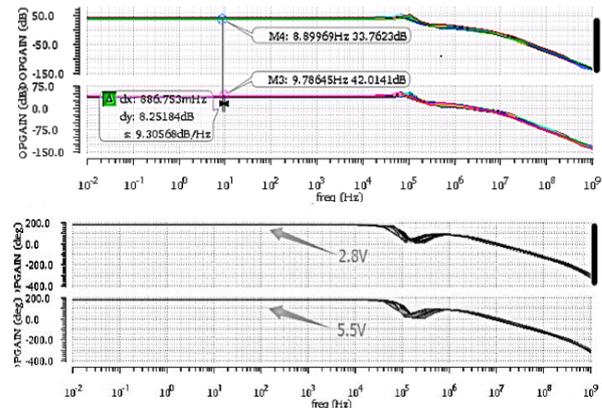
Figure 7. Bode plot of reference voltage source circuit

The variation of the reference voltage due to random errors is shown in Figure 7.
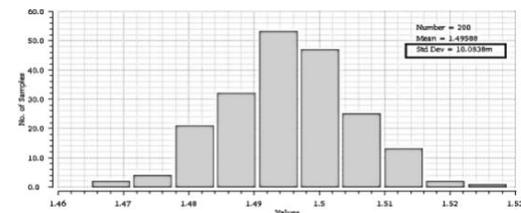
Figure 8. Reference voltage monte carlo simulation

The Monte Carlo simulation reflects the mismatch characteristics of the devices during the manufacturing process. The change from the reference voltage is 2%.

5.2 Simulation and Analysis of High-precision current sense circuit

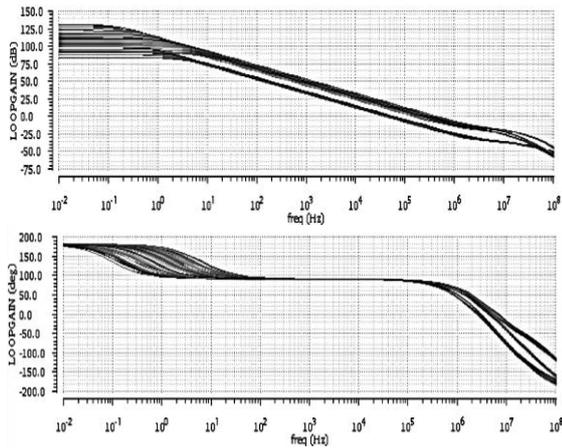According to the data analysis in Figure 8, high-precision current sense circuit is stable.

Figure 9. Bode plot of high-precision current detecte circuit

The normal distribution of the Monte Carlo simulation is shown in Figure 9. In order to verify that the circuit can meet the accuracy required after adjustment, the measured voltage must be compared with the desired reference voltage, by converting the analog quantity into digital quantity. The MC simulation of the current detection circuit after trimming is shown in Figure 10, and the detection accuracy increased by 5.55% .
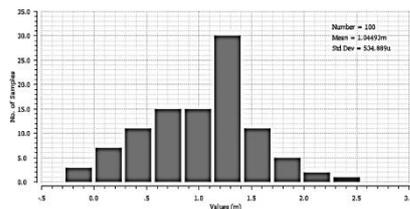

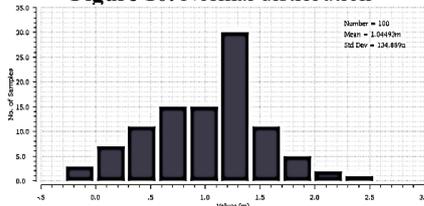**Figure 10.** Normal distribution

Figure 11. Normal distribution after trimming

References

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