Design of bootstrap integrated synchronous rectifier

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Abstract. Based on the research of the development of synchronous rectification technology, this paper proposes a circuit structure of bootstrap synchronous rectifier chip. Firstly, through the research of synchronous rectification technology, the architecture of synchronous rectification chip is determined. After the system design is completed, the internal units of the chip are designed in blocks under the 0.35 μm BCD process, and the specific circuit design is completed. Each unit has been verified by HSPICE simulation and has reached the specified index. The system constructed by this has also been verified by simulation, and the simulation results are consistent with the expected results, indicating that the main design functions of the circuit have been realized.

1 Introduction

In the modern low-voltage and high-current switching power supply, the loss of the rectifier diode has occupied a large part of the total power loss. In order to solve this problem synchronous rectification technology was proposed, which is based on the new MOS manufacturing technology at the ending of the last century. Synchronous rectification technology is a technology that uses a dedicated MOSFET with a small on-resistance to replace the Schottky rectifier diode to reduce the rectification loss. In order to reduce the power consumption of the flyback converter output rectifier diode and improve the efficiency of the flyback power supply, synchronous rectification technology is also required. In synchronous rectification technology, the synchronous rectification drive mode is very important. In terms of dedicated drive circuits, several synchronous rectification driver chips have been developed to improve the safety and reliability of the system. However, the prior art synchronous rectifying circuit has more pin and complicated external connection. In practical application, the less is the number of connection pins, the lower are the costs of the circuit.

In order to solve this problem, this paper proposes a Bootstrap synchronous rectification driver circuit. The structure is simplified so that the required area on the print circuit board is reduced and the cost of the power supply is decreased.

The driver chip is mainly used to drive the synchronous rectifier MOSFET of the flyback converter operating in DCM or quasi-resonant mode. At the same time, the driver chip does not require additional devices. By detecting the change of the drain voltage of the rectifying MOSFET, the state of the primary side switching MOSFET can be automatically and accurately determined to achieve synchronous driving.

2 Bootstrap synchronous rectification driver chip

2.1 Specification

Since the driver chip designed in this paper is mainly applied to adapters of consumer and office electronics products such as notebooks and mobile phone. The power supply input voltage range of the driver chip is 20 ~ 60V. The wide input power supply voltage range makes the chip wider. The VCC supply supplies power to the LDO and output modules. Therefore, the VCC voltage is 9 ~ 11V; The undervoltage lockout threshold is 3.5V ~ 4.5V; the output drive rectifier MOSFET voltage is 8 ~ 10V; after the primary switch is turned off, to prevent punch through, set the rectifier MOSFET turn-on delay to 300ns.

2.2 Architecture of The Chip

The block diagram of the chip is shown in Figure 1. At power-on, the VCC is powered by internal self-power. When the VCC voltage is lower than 5V, the built-in power MOSFET is turned off, and the parasitic body diode of the power MOSFET is electrically conductive. When the VCC voltage reaches 5V, the synchronous rectification circuit is activated.
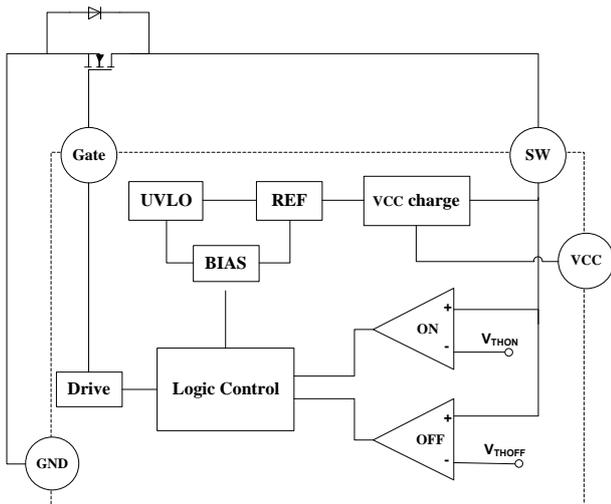
Figure 1. Architecture of the chip

The circuit detects the V_{DS} voltage through the SW pin. When the V_{DS} voltage is lower than the threshold of V_{THON}, a driving signal is generated inside the circuit to drive the internal MOSFET to conduct after a certain delay. At this time, the current is immediately transferred from the internal parasitic diode to turn on the MOSFET. As the energy stored in the transformer is slowly released, the current through the MOSFET will also slowly decrease to zero, and the voltage of V_{DS} will also rise slowly. When the SW pin detects that the V_{DS} voltage is higher than the threshold of V_{THOFF}, the driving voltage is turned off after a certain delay, and the MOSFET enters the off state again.

2.3 The Key Unit

The VCC charge unit of synchronous rectifier chip designed in this paper is shown in Figure 2. When the primary switching transistor is turned on, the rectifier MOSFET is turned off. At this time, the SW pin is charged by the auxiliary capacitor to charge the external capacitor of the VCC pin, and is charged to a predetermined voltage value before the primary switching transistor is turned off. By designing the threshold of the OVP circuit, the Logic circuit controls the turn-on and turn-off of P0 to stabilize VCC between 9 and 11V.
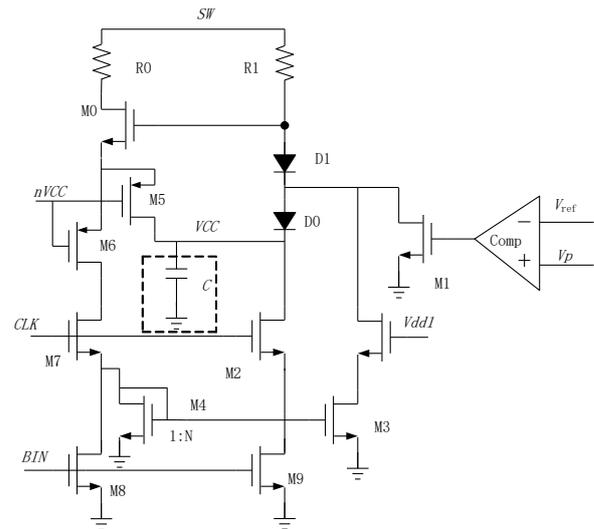

Figure 2. VCC charge unit

The logic control unit of synchronous rectifier chip designed in this paper is shown in Figure 3. It is mainly composed of RS flip-flop and delay logic gate circuit. The logic control module process OFF signal, ON signal, UVLO signal and SWSA signal, then output the correct gate pulse drive signal DRIVE to turn the SR MOS on or off.
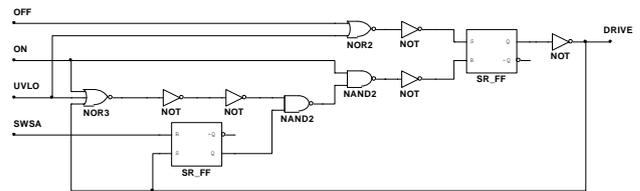

Figure 3. Logic control unit

The drive unit structure of the synchronous rectification integrated circuit designed in this paper is shown in Figure 3. When the DRIVE signal is high, the driving circuit pulls the rectifier MOSFET gate voltage to 10V. When the DRIVE signal is low, the driving circuit pulls the rectifier MOSFET gate voltage to the ground potential. By controlling the VLO signal, the rectifier MOSFET can be quickly turned off.
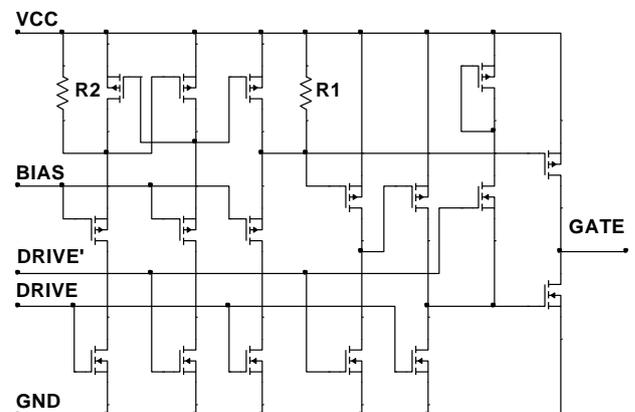

Figure 4. Drive unit

3 Simulation

3.1 Simulation of VCC Charge Unit

Figure 5 shows the voltage waveform of the charge unit. It can be seen from the figure that the startup time of the system is 1.05 ms. After a short startup process, the auxiliary power supply VCC reaches a steady state, and output voltage is 10V. It indicates that the startup circuit can work normally, and the auxiliary power supply can provide a stable voltage inside.
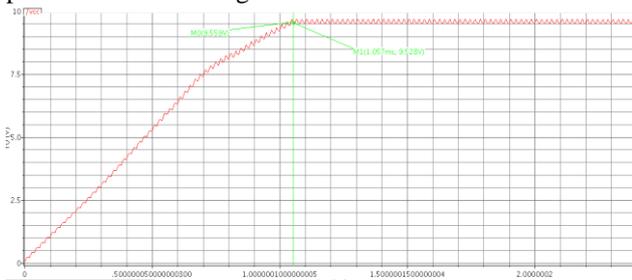

Figure 5. Simulation of charge unit

3.2 Simulation of Logic Control Unit

Figure 6 shows the transient simulation results of the designed logic control circuit. As shown in the figure6, when UVLO is high, it enters the undervoltage protection state and DRIVE is low. When UVLO is low, SR_ON generates turn-on pulse at 19.527 ms and 19.547 ms, and SR_OFF generates a turn-off pulse at 19.537 ms and 19.557 ms. The false turn-on signal at 19.558 ms and the false turn-off signal at 19.539 ms are ignored.
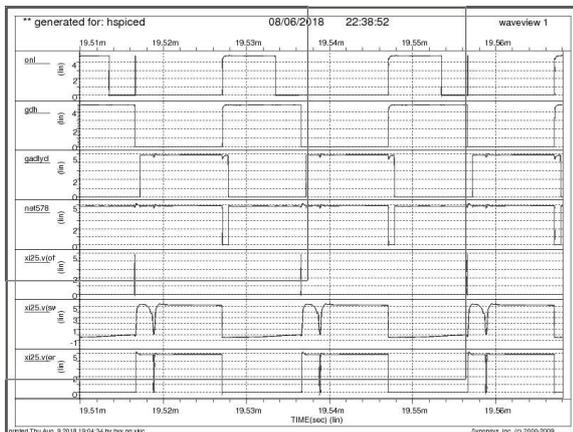

Figure 6. Simulation of logic control unit

3.3 Simulation of Synchronous Rectifier Flyback Converter System

The system simulation model shown in Figure 7 is used to verify that the chip meets design requirements. The parameters are as follows: the input voltage is 85V, the output voltage is 25V, the output current is 0.25A, the switching frequency is 50 kHz, the primary inductance of the transformer is 2.44 mH, and the turns ratio is 2.94.
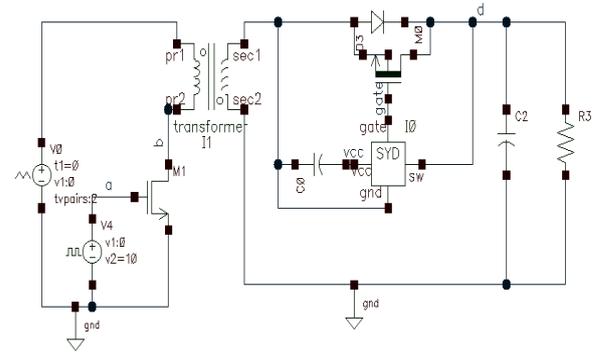

Figure 7. System function simulation circuit schematic

It can be seen from the simulation waveform in Figure 4.5 that after the primary MOSFET is turned off, the body diode of the rectifier MOSFET is turned on first, and the drain voltage of the rectifier MOSFET becomes negative. After the chip detects this voltage change process, the drive signal goes high, turning the rectifier MOSFET on, and the turn-on delay is 360.18ns. After the rectifier MOSFET is turned on, the current of the rectifier MOSFET begins to increase rapidly, and the current of the body diode begins to rapidly decrease to zero. After that, the MOSFET current slowly decreases. When the current of the rectifier MOSFET is detected to drop to 4.65mA, the drive signal goes low, and the rectifier MOSFET is quickly turned off. After the delay, the primary MOSFET begins to conduct. The chip is prevented from accidentally turning on the rectifier MOSFET due to the detection of the resonant signal of the gate drive signal. This shows that the system can normally detect the change of the rectified MOSFET drain voltage and generate an appropriate drive signal.
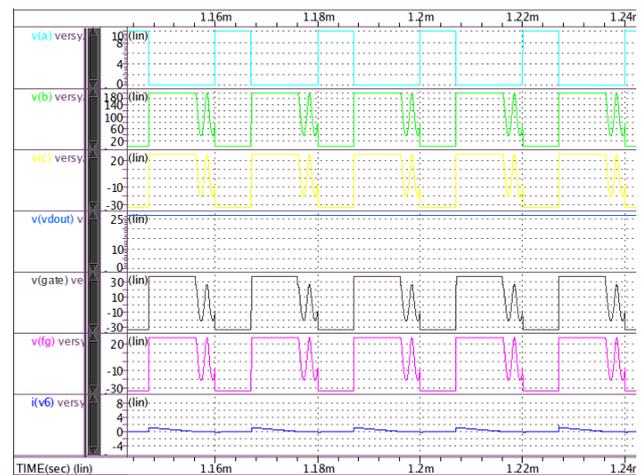

Figure 8. Simulation of synchronous rectifier flyback converter

4 Conclusion

In this paper, the circuit structure of a bootstrap synchronous rectifier chip is proposed, which makes the chip have the characteristics of less pins and simple external connection. This paper determines the architecture of the synchronous rectifier chip and designs the internal unit circuits inside the chip. The unit circuit

and its typical application circuit are simulated by 0.35 μm BCD process parameters. The simulation results show that the driver chip obtains the state of the primary MOSFET by sampling the rectifier MOSFET drain voltage. After the primary MOSFET is turned off, the rectifier MOSFET drain voltage is extremely negative with respect to the source. At this time, the rectifier MOSFET is turned on to realize the synchronous rectification function. When the energy stored in the transformer is about to be fully discharged, the drain voltage is almost equal to the source voltage, and the rectifier MOSFET transistor is turned off. From the results of the simulation, the designed chip meets the requirements.

References

1. Ta-yung Yang, Jun-jie Kuo, Tso Min Chen. PWM controller for synchorous rectifier of flyback power converter[P]. US Patent: 0018135A1, 2006-01-26.
2. Piyush Bhardwaj, Kowsalya M.A. Dual Output Flyback Converter for Photovoltaic Applications[C]. IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems, 2016: 1-5.
3. Wei Yuan, X. C. Huang, J. M. Zhang, Z. M. Qian.A Novel Soft Switching Flyback Converter with Synchronous Rectification[C]. IPEMC, 2009: 551-555.
4. Park J, Roh Y S, Moon Y J, et al. A CCM/DCM Dual-Mode Synchronous Rectification Controller for a High-Efficiency Flyback Converter[J]. IEEE Transactions on Power Electronics, 2013, 29(2): 768-774.
5. Hasegawa M, Matsumoto T, Nagai R. Control circuit for synchronous rectifier-type DC-DC converter, synchronous rectifier-type DC-DC converter and control method thereof: US, US7843179[P]. 2010.