4.5kV FRD Development for high current power modules

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Abstract. A 4.5kV/100A FRD was designed by simulation, which had optimized carrier density distribute cell and ruggedness terminal. The cell was composed of P-body/N-sub/N+ layers, when the P-body doping concentration is lower, the carrier density distribution on the P-body/N-sub is lower; when carrier density di stribution on the P-body/N-sub side is lower than that on the N-sub/N+ side, the FRD has soft recovery but bad surge-current capability. So the P-body doping concentration needs trade-off consideration. Lifetime co ntrol technology was also used to optimize the carrier density distribution and trade-off characteristics. The t erminal has high breakdown voltage, low electric field and large process window, which means more rugge dness and high reliability. The experiment results show that the design chip and competitor chip has nearly t he same trade-off characteristics, the design chip has larger dynamic loss but lower static loss. The design c hip has high surge current, the surge current is 13 times as much as the rate current.

1 Introduction

Fast Recovery Diodes (FRD) is usually used as free-wheeling diode in anti-parallel to the IGBTs, which is an effective solution for easier controlled in the field of power systems. The low losses and soft switching behaviour of the diode attract the most attention. It requires current ratings of 50A to 300A per chip and blocking voltages in the range of 1.7kV to 6.5kV in power system applications. The working frequency of the chips in power system applications is in the range of 100Hz to 15kHz. The chips can be used for Flexible Alternating Current Transmission Systems (FACTS), DC circuit breaker and High-Voltage Direct Current (HVDC), etc. The device with lower conduction voltage can effectively reduce the loss of the conduction, thus the total loss is diminished. The applications also require reverse recovery softness, high ruggedness and good surge-current capability.

During the past two decades, a lot of studies have been done in the field of FRDs. It has been demonstrated that several concepts (such as CIBH, FCE) offer a significantly improved characteristics [1-3]. However, it is difficult to optimize the trade-off characteristics. In this paper, optimized structure and lifetime were proposed, the anode emission efficiency was optimized and carrier lifetime was killed by lifetime control technology. The experiment show low conduction loss, soft reverse recovery and good surge-current capability.

2 Structure design

The 4.5kV/100A diode cell structure is shown in Fig.1. It is composed of P-body/N-sub/N+ layers, the P-body contact with the anode electrode, and the N+ contact with the cathode electrode.

The three layer thickness and doping profile need careful consideration to get low loss, high ruggedness and good surge-current capability. The optimized P-body peak concentration is 2E17/cm3 and depth is about 10μm. The N-sub doping concentration is about 1E13/cm^3, 430ohm.cm, and thickness is 500μm. The N+ peak concentration is near 1E20/cm^3 and depth is about 40μm. It's important to point out that the surface of P-body has higher doping nearly 1E19/cm^3 to ensure ohm contact.

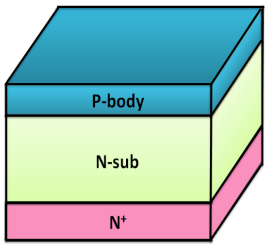

Figure 1. Schematic cross sections of cell

The 4.5kV/100A diode terminal structure is shown in Fig.2. It is composed of multi-deep P-rings (PRs) and total dimension is about 1.8mm. The PR width, PR space and passivation process needs optimization.

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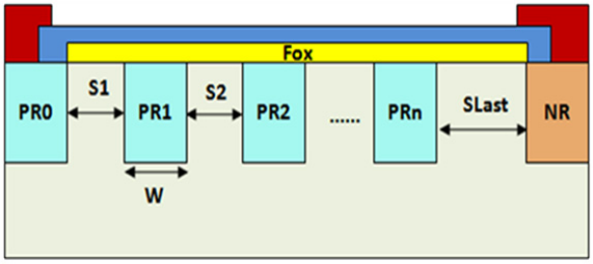

Figure 2. Schematic cross sections of terminal

2.1 Cell design

The cell characteristic was determined by carrier density distribution. When carrier density distribution on the P-body/N-sub side is lower than carrier density distribution on the N-sub/N+ side, the FRD has soft recovery [4-6]. The removal of the plasma will start more rapidly at the P-body/N-sub junction than at the N-sub/N+ junction, and result in the final plasma remains within the N-sub region near N-sub/N+ junction and soft recovery[7].

The carrier density distribution on the P-body/N-sub side depends on the P-body doping concentration. When the P-body doping concentration increases, the carrier density increases, the conduction loss is lower but has bad surge-current capability, vice versa. So P-body doping concentration needs carefully consideration. Lifetime control technology was also used to optimize the carrier density distribution and trade-off characteristics.

Fig.3 shows simulation result of 4.5kV/100A diode reverse recovery behaviour, which has a soft recovery. The peak reverse recovery current is about 120A, a little more than rated current.

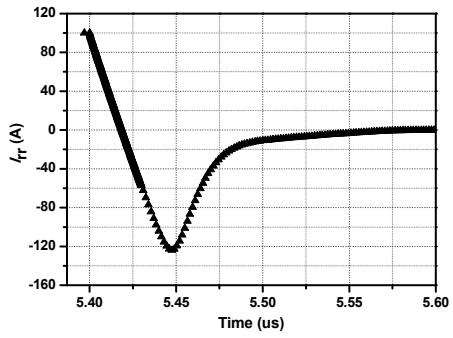

Figure 3. Simulated current profiles under reverse recovery conditions (Conditions: V_R=2.8kV, I_F=100A, di/dt=600A/us, T_j=25°C)

Fig.4 shows the holes density distribution during the reverse recovery time. The cathode side has remained holes at tail time, lead to soft reverse recovery behaviour. It's important to point out that Fig.4 t=0μs is corresponding to Fig.3 t=5.4μs.

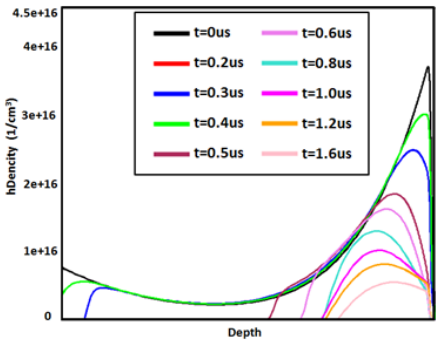

Figure 4. The simulated holes density distribution during the reverse recovery time

2.2 Terminal design

Fig.5 shows the breakdown voltage of the terminal, the breakdown voltage exceeds 6000V and is more than 1.3 times as much as rated voltage. The high voltage margin results in high reliability.

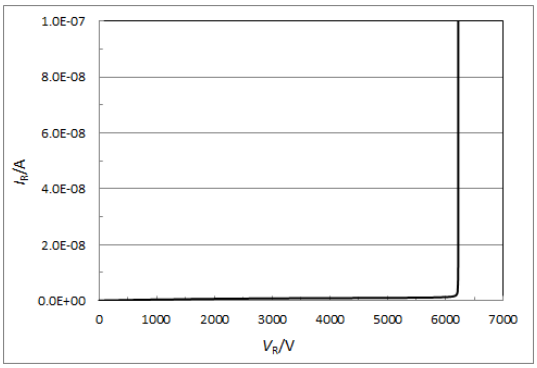

Figure 5. The breakdown voltage of terminal

Fig.6 shows the electric field distribution of terminal at breakdown voltage, the peak electric field was on the middle of the terminal and was lower than 2.1E5V/cm. The low peak electric field and parabolic electric field profile lead to more ruggedness and high reliability.

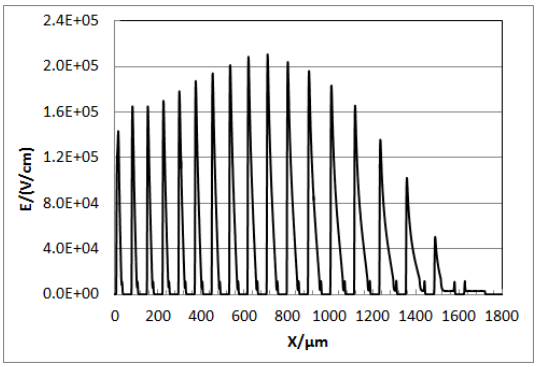

Figure 6. The simulated electric field of terminal

Table.1-3 show window check simulation result of terminal. Along with PR dosage and N substrate doping concentration decrease, the breakdown voltage increase. The PR width vary 4μm has no obvious effect on breakdown voltage.

Table 1. The breakdown voltage against different dose of P-ring

PR dose(cm^{-2})	Breakdown voltage（V）
3.00E+13	5800
6.00E+13	5960
1.00E+14	6275

Table 2. The breakdown voltage against different N-sub doping concentration

N-sub concentration (cm^{-3})	Breakdown voltage（V）
Sub+20%	5810
Sub	6275
Sub-20%	6730

Table 3. The breakdown voltage against different width of P-ring

PR width (μm)	Breakdown voltage（V）
W-4	6258
W	6275
W+4	6267

3 Experiment Results

The 4.5kV/100A FRD chip was fabricated base on the simulation. After fine-tune the process, especial lifetime control condition, the static and dynamic characteristics meet the design target.

Fig.7 shows the optics microscope picture of 4.5kV /100A FRD wafer.

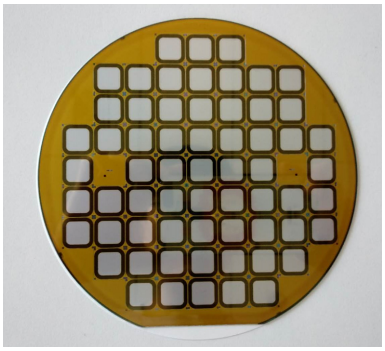

Figure 7. Optics microscope picture of 4.5kV/100A FRD wafer

Fig.8 shows the breakdown voltage mapping test result, the voltage was about 6150V, meet the simulation result.

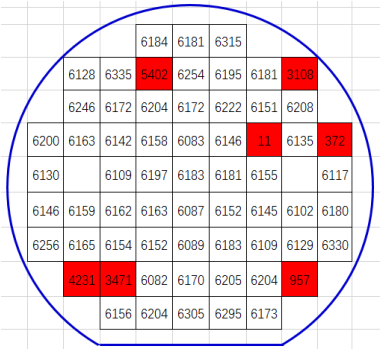

Figure 8. Experiment breakdown voltage mapping data. (Conditions: I_r=1mA, T_j=25℃)

Table 4 shows the static characteristics between the design chip and a competitor chip. The design chip forward voltage was lower than competitor and the reverse leakage current was on the same lever.

Table 4. Static characteristics comparison between own design and competitor chip

Characteristics	V_f/V		I_r/μA	I_r/mA
Bias	100A		4500V	
Temperature/℃	25	125	25	125
Design chip	2.46	2.68	0	0.75
Competitor chip	2.82	3.06	0	1.10

Table 5 shows the dynamic characteristics between the design chip and a competitor chip. The design chip dynamic characteristic was larger than competitor.

The design chip and competitor chip has nearly the same trade-off characteristic, the design chip has larger dynamic characteristic but lower static characteristic.

Table 5. Dynamic characteristics comparison between own design and competitor chip

Characteristics	I_{RM}/A		Q_{rr}/μC		T_{rr}/μs		E_{rec}/mJ	
Bias	V_R=2800V,V_{GE}=+/-15V							
Temperature/°C	25	125	25	125	25	125	25	125
Design chip	150	154	50	62	0.60	0.75	22	27
Competitor chip	109	129	32	48	0.50	0.67	14	22

Fig.9 and Fig.10 shows design chip has soft reverse recovery behaviour at room and high temperature.

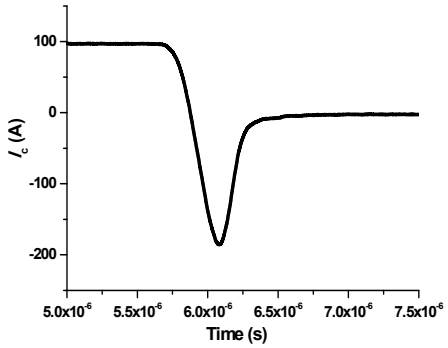

Figure 9. Experiment current profiles under reverse recovery conditions. (Conditions: V_R=2.8kV, I_F=100A, *di/dt*=600A/us, T_j=25℃)

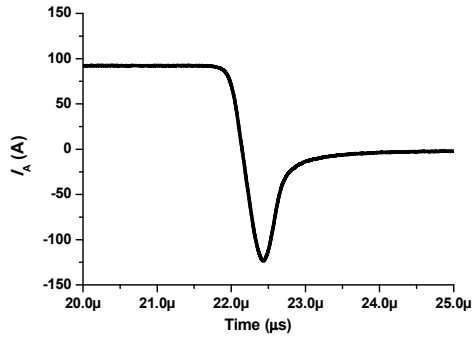

Figure 10. Experiment current profiles under reverse recovery conditions. (Conditions: V_R=2.8kV, I_F=100A, *di/dt*=600A/us, T_j=125℃)

The design chip also has high surge current, the surge current is 13 times as much as the rate current.

4 Conclusions

In conclusion, a 4.5kV/100A FRD was designed with the aid of simulation tools and verified by experiment.

The FRD trade-off characteristics were determined by the carrier density distribution. Low concentration P-body doping lead to soft recovery but had surge-current capability, so P-body doping concentration need trade-off consideration. Lifetime control technology is also a useful tool to optimize the carrier density distribution. The terminal simulation results show high breakdown voltage, low electric field and large process window, which mean more ruggedness and high reliability.

This device was fabricated and the test results show that the design chip and competitor chip has nearly the same trade-off characteristics, the design chip has larger dynamic loss but lower static loss. The design chip also has high surge current, the surge current is 13 times as much as the rate current.

Acknowledgment

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