

Solution for the Drift Problem of the Chip in the Packaging Process

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Abstract. This paper analyzes the drift phenomenon of the chips appearing in the packaging process of the fast recovery diode (FRD), and proposes an effective process to solve this problem. In order to improve the trade-off characteristics of fast recovery diodes, lifetime control methods, such as electron irradiation, high-energy ion implantation and so on, are often introduced in the chip manufacturing process. The chips described in this paper use the lifetime control method of electron irradiation. The problem of chips drift during the packaging process has been found. In this paper, by comparing different back metal schemes, comparing and analyzing the products of different manufacturers, the cause of chips drift is ultimately located in the annealing process after electron irradiation. The result of this paper shows that the chips drift phenomenon can be solved by adjusting the process steps.

1 Introduction

Fast Recovery Diode (FRD) is a diode with a short reverse recovery process and is usually characterized by the parameter of reverse recovery time (t_{rr})^[1]. The FRD is usually used in anti-parallel with the IGBT and works together in a high-voltage, high-frequency environment. This puts higher requirements on the diode. The diode need to have faster reverse recovery time, lower leakage current and softer reverse recovery characteristics^[2].

In order to shorten the reverse recovery time, the lifetime control method is usually adopted. Different deep level recombination centers are introduced in the bandgap to reduce the lifetime of minority carriers, thereby accelerating the reverse recovery of the device. In this paper, the global lifetime control technology of electron irradiation is used to shorten the reverse recovery time of the device. It uses an electron beam with an energy of 0.15~15MHz to penetrate the whole device, which can uniformly induce point defects inside the chip to form a composite center. In this way, the lifetime of excess carrier is controlled^[3]. In order to remove unstable defects, the annealing is performed at a certain temperature after electron irradiation. Some defects caused by electron irradiation in silicon materials are disappeared immediately at the end of irradiation^[4]. Some defects are combined under the action of annealing. Secondary defects with higher temperature resistance may also occur during annealing^[5]. By annealing, a stable recombination center can be retained.

2 Analysis of Chips Drift

2.1 Introduction to the packaging scheme and problems in the packaging process

The chips of batch 1 were manufactured by foundry 1. The static parameters were normal in the CP test, so those chips were subjected to subsequent package test verification. The package test plan is shown in Table 1 below.

Table 1. Plan of package and test

Package form	FRD Wafer		Number of package modules	Static test	Dynamic test
	Batch	Wafer number			
T1V	1	6#/13#	6#: 40 modules 13#: 2 modules	Do	Do
	6#/13#				

Reflow soldering^[6] is one of packaging processes. Feedback from the packaging factory was that the chips have drifted during the reflow soldering process, as shown in Figure 1.

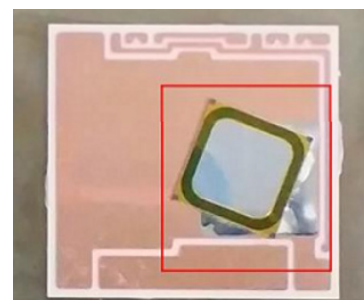


Figure 1. Chips drift during reflow soldering

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2.2 Troubleshoot the packaging process

In response to the above problem, 4 diodes were selected for shear and tensile testing, the results are shown in Table 2.

Table 2. Shear and tensile testing

ITEM	Shear test		Pull test	
	15mil		15mil	
Wire Size	diode 1	diode 2	diode 3	diode 4
X1	1749.4	1439.9	917.1	1033
X2	1589.3	1462.5	962.7	1078.8
X3	1575	1462	1020	979.3
X4	1908.7	1593.4	999.7	1071.1
X5	1827.8	1704.4	1024.6	1009.3
X6	1771.4	1667.8	963.2	937.7
X7	1840.1	1417	1074.7	929
X8	1881.1	1541.1	1049.5	850.6
X9	1939.7	1445	992.2	919
X10	1847.9	1617.9	999.7	862.2
LSL	750	750	500	500
AVE	1793.04	1535.1	1000.34	967
MAX	1939.7	1704.4	1074.7	1078.8
MIN	1575	1417	917.1	850.6
STD	124.9434	104.5124	45.59886	80.80919
PPK	2.7827	2.50401	3.657548	1.926349

It was found that the test values met the requirements, which indicates that although the chips had drift phenomenon, the chips were well soldered on the composite copper plate.

In order to further check whether the drift of the chips were related to the packaging process, four chips produced by two foundries were selected. These four chips are divided into two groups according to the different foundries. These four chips were packaged by the same packaging process.

The test comparison results are shown in Figure 2. Drift occurred in the two chips produced by foundry 1. The two chips of the foundry 2 were normal. It can be confirmed that the drift of the chips should be independent of the packaging process.

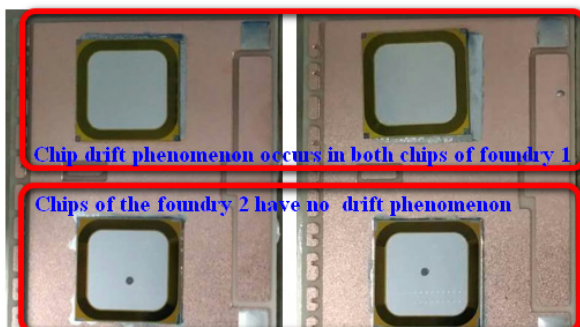


Figure2. Chips drift performance of different foundries

2.3 Troubleshoot the back metal

After excluding the problem of the packaging process, it was suspected that the back metal caused the phenomenon of chips drift. By adjusting the ratio of the back metals or replacing the back metals composition, four back metal schemes were developed.

First, a group experiment was conducted on the backside metal process of the chips. The result is shown in Table 3. It shows that the chips drift regardless of the back metal scheme.

Table 3. Effect of different back metal schemes on chips drift

Foundry number	Wafer No	Back metal condition	Whether the chips drift
Foundry 1	2#	Scheme 1	Yes
	3#	Scheme 2	Yes
	5#	Scheme 3	Yes
	7#	Scheme 4	Yes

Next, the performance of two foundries of chips with identical backside metal process was compared. It was found that all the chips manufactured by foundry 1 had drift phenomenon. However, the chips manufactured in the foundry 2 with the same backside metal process conditions had no drift phenomenon.

Table 4. Comparison of chips drift phenomenon in different foundries

Foundry	Back metal condition	Whether the chips drift
Foundry 1	Scheme 1	Yes
Foundry 2	Scheme 1	No

At this point, the backside metal process which suspected leading to the chips drift in the packaging process can be preliminarily ruled out.

2.4 Positioning the cause of chips drift

After excluding the problem of the backside metal leading to chips drift, lifetime control treatment became a suspect. After the backside metal process, the chips produced by the foundry 1 were subjected to electron irradiation and furnace tube annealing^[6]. Oxygen atmosphere may be introduced during annealing of furnace tube. This may cause oxidation of the metal on the backside of the chip. Oxidized metal will not stick to tin, which leads to chips drift.

To verify the speculation, twelve chips which were produced by foundry 1 were selected. In the batch 1/2/3, each of the 4 chips were selected for the adhesion test of the back metal. In the batch 1 of the 4 chips, the electron irradiation and furnace tube annealing method was used for lifetime control. The batch 2 of 4 chips did not have lifetime control. The batch 3 of 4 chips, the lifetime control was carried out by means of electron irradiation and vacuum annealing^[7]. The advantage of vacuum annealing over furnace tube annealing is that the atmosphere contains no oxygen and there is no need to worry about the metal oxidation during the annealing process. The other processes of the three batches were identical. The comparison results are shown in Table 5. The situation of sticking tin is shown in Figure 3.

From the comparison results, it can be preliminarily speculated that the backside metal was oxidized due to furnace tube annealing after electron irradiation.

Oxidized metal was not stick to tin, which led to chips drift.

Table 5. Comparison of results of the stick tin experiment

Batch No	Chip No	Lifetime control	Whether metal stick to tin
Batch1	#1	Electron irradiation + Furnace tube annealing	No
Batch1	#2	Electron irradiation + Furnace tube annealing	No
Batch1	#3	Electron irradiation + Furnace tube annealing	No
Batch1	#4	Electron irradiation + Furnace tube annealing	No
Batch2	#1	No	Yes
Batch2	#2	No	Yes
Batch2	#3	No	Yes
Batch2	#4	No	Yes
Batch3	#1	Electron irradiation + Vacuum annealing	Yes
Batch3	#2	Electron irradiation + Vacuum annealing	Yes
Batch3	#3	Electron irradiation + Vacuum annealing	Yes
Batch3	#4	Electron irradiation + Vacuum annealing	Yes



Figure 3. Situation of sticking tin

3 Process step adjustment

To solve this problem, vacuum annealing can be selected. However, due to the limitations of foundry 1, the way of annealing was difficult to change. In the next batch, the process steps were adjusted, and the electron irradiation and furnace tube annealing was mentioned before the backside metal process. The specific process steps are as follows:

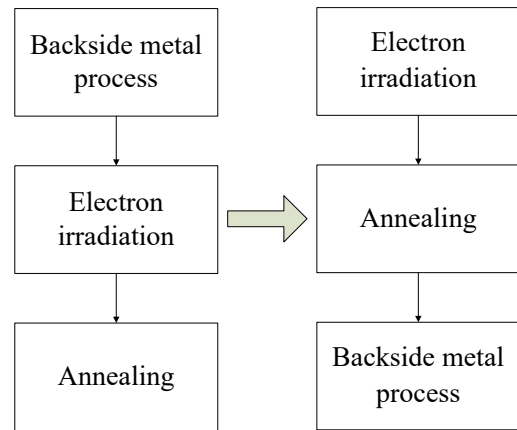


Figure 4. Process step adjustment

These chips have been packaged at present, and the chips have no drift phenomenon. The result is shown in Figure 5.



Figure 5. The result of chips drift phenomenon

After the packaging process, some modules were selected for High Temperature Reverse Bias (HTRB)^[8] test, and the modules passed 168h successfully. The results are shown in Table 6.

Table 6. The results of HTRB

Package number	Module number	Before HTRB		After 168h HTRB	
		V _F /V	I _R /uA	V _F /V	I _R /uA
Y319	#3-7	2.07	17	2.2	31
	#3-8	2.06	17	2.47	41
	#3-9	2.06	17	2.55	53
	#3-10	2.07	17	2.53	40

At this point, by adjusting the relevant process steps, the drift problem of the FRD chips in the packaging process was solved.

4 Conclusions

This paper starts with the chips drift problem in the packaging process, gradually eliminates the related problems, and finally locates the problem of the backside metal oxidation of the chip. The root cause of this problem comes from furnace tube annealing in the lifetime control process. Oxygen in the atmosphere during annealing of the tube causes oxidation of the backside metal. The chips drift problem has been effectively solved by adjusting the electron irradiation and furnace tube annealing to the back metal process.

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References

1. CHEN Zuliang, YUE Wei, LI Zhaolong, et al. Improvement of reverse breakdown characteristics of bipolar switching transistors by electron irradiation[J]. *Semiconductor Technology*, 2014, 39(12): 943-946.
2. Siemieniec R, Südkamp W, Lutz J. Determination of parameters of radiation induced traps in silicon[J]. *Solid State Electronics*, 2002, 46(6):891-901.F. De Lillo, F. Cecconi, G. Lacorata, A. Vulpiani, *EPL*, 84 (2008)
3. MEN Yongjuan, WANG Chuanmin. Effect of Platinum and Gold Doping on the Performance of Fast Recovery Diodes[J]. *Power Electronics*, 2010(6): 60-62.
4. Chen Panxun. Radiation effects of semiconductor devices and integrated circuits [M]. National Defence Industry Press, 2005.
5. Zhong Zhiqin. Study on the Irradiation Effect of 6H-SiC [D]. Sichuan University, 2007.
6. Guan Guozhi, Xing Zhongyan. Application of Infrared Finger Heater in Boiler Tube Annealing[J]. *Petroleum Construction Technology*, 1983(2): 38-41.
7. Xiao-Bin L I, Ding L, Guo J X, et al. Modeling and optimization for vacuum annealing furnace[J]. *Control & Decision*, 2005, 20(2).
8. Dong Shaohua, Liu Yuyang, He Yanqiang, et al. HTRB test method and phenomenon research [J]. *Smart Grid*, 2016, 4(12):1200-1203.