

# Design of Oscillator Based on A Deformed Structure Parallel Coupled Line Filter

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**Abstract.** This paper proposes an oscillator based on a deformed structure parallel coupled line filter design. The requirements of this design are the output power meet 10dBm, and phase noise is below -90dBc/Hz at 10kHz off the centre point. This work adopts parallel positive feedback form, and it use Parallel Coupled Line Filter, making this design simple in structure and low in cost. This design has low phase noise and high output power features, working at 2.4GHz, intended to use in a through-the-wall radar system.

## 1 Introduction

As an important part of microwave circuit system, the oscillator is one of the most exploited and ubiquitous modules in Radio Frequency Integrated Circuit (RFIC) systems which have to comply with stringent requirements. And its performance often determines whether the entire system will meet specifications or not. Output power, phase noise and harmonic suppression are critical parameters of an oscillator [1].

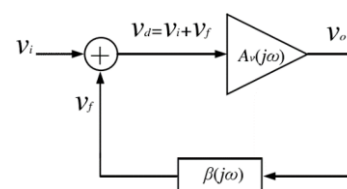
Oscillators are normally comprised of two distinct sections, namely, the active section, and the resonator, which a device that naturally oscillates at a certain frequency. There are many kinds of resonator, for example, LC tank, crystal, surface acoustic wave, yttrium iron garnet and dielectric resonators. In many studies, parallel coupled line filters have been widely used due to their simple structure and low cost. In recent years, substrate integrated waveguides with higher  $Q$  values have also attracted the attention and application of many scholars. And many research working on the low phase noise oscillators and their behavior has been down [2-5].

When the software ADS is used for schematic simulation, its results are under ideal original conditions, which is different from the actual one. The electromagnetic simulation (EM simulation) compares the layout of the analog circuit on the dielectric substrate and the result of the component package with parasitic parameters to obtain simulation data that is closer to the actual situation.

This paper proposes an oscillator which has low phase noise and high output power, working at 2.4GHz, intended to use in a through-the-wall radar system. And this paper will introduce the design of the oscillator from two aspects, low noise amplifier and parallel coupled line filter. Then analyze the results of EM and schematic co-simulation and discuss about the results of it.

## 2 Design of oscillator

Parallel feedback oscillators are based on positive feedback system. Part of the transistor output signal is fed back to the transistor input end through the feedback loop. When this part of signal is in phase with the transistor input signal, the oscillating circuit works in positive feedback state. When satisfying certain starting conditions and maintaining oscillation conditions, the output of the transistor will produce a stable output signal. The schematic diagram of parallel feedback oscillator is shown in Figure 1.



**Figure 1.** Schematic diagram of parallel feedback oscillator

$A_v(j\omega)$  represents the voltage amplification factor before the transistor access loop, which is the open loop gain.  $\beta(j\omega)$  represents a ratio of  $v_f$  to  $v_o$ , which is the transmission coefficient of the feedback network.

$$v_o = A_v(j\omega) \cdot v_d \quad (1)$$

$$v_f = \beta(j\omega) \cdot v_o \quad (2)$$

As for parallel feedback oscillators, according to Barkhausen Criterion, we must ensure that the loop is a positive feedback state and the whole loop gain is 1. Let us define  $A_{vf}(j\omega)$  as Closed loop voltage gain:

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$$A_{vf}(j\omega) = \frac{v_o}{v_i} = \frac{A_v(j\omega)}{1 - \beta(j\omega)A_v(j\omega)} \quad (3)$$

Based on the above analysis, we can draw a conclusion [6]:

$$|\beta(j\omega)A_v(j\omega)| = 1 \quad (4)$$

$$\arg(\beta(j\omega)A_v(j\omega)) = \pm n \cdot 360^\circ, n = 0, 1, 2, \dots \quad (5)$$

## 2.1 Low noise amplifier

Since the designed oscillator needs higher output power, considering Field Effect Tube(FET) has better noise factor but lower max gain, this work chooses Bipolar Junction Transistor(BJT) BFP520 to implement active amplifier part. By consulting the datasheet of BFP520, this work adopts co emitter structure, setting the Bias point at  $V_{ce} = 2V, I_c = 20mA$ .

In order to make the transistor work steadily and in the state of amplify, this work verifies the stability factor  $K$  working at above Bias point by following formulate [7].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2 \cdot |S_{12}| \cdot |S_{21}|} > 1 \quad (6)$$

$$D = S_{11} \cdot S_{22} - S_{12} \cdot S_{21} \quad (7)$$

$$|S_{12}| \cdot |S_{21}| < 1 - |S_{11}|^2 \quad (8)$$

$$|S_{12}| \cdot |S_{21}| < 1 - |S_{22}|^2 \quad (9)$$

The next step is to match input and output impedance. In order to make the load absorb the maximum power, the input and output terminals are both conjugate matched. However, in order to reduce the phase noise, the matching of the input ends is based on the minimum noise impedance matching, matching input impedance  $Z_{in}$  of the LNA to Conjugate source impedance  $Z_s^*$ , by entering matching network.

$$Z_{in}(z) = Z_0 \cdot \frac{Z_L + jZ_0 \cdot \tan \beta z}{Z_0 + jZ_L \cdot \tan \beta z} \quad (10)$$

And the matching of the output ends is based on the maximum gain impedance matching. The schematic diagram of impedance matching is shown as figure2.

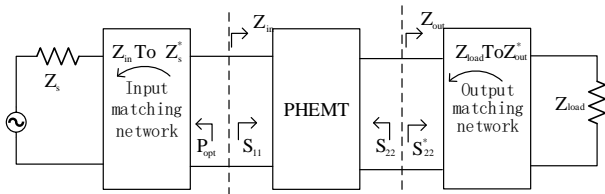


Figure 2. Schematic diagram of impedance matching

## 2.2 Parallel coupled micro strip line filter

In [8], the author proposed the design procedure of micro strip parallel coupled-line band-pass filters for multi-

spurious pass-band suppression. These parameters could be represented by an equivalent circuit of the admittance inverter  $J$  and a single line of two electrical lengths of  $\theta$  and admittance  $Y_n (n = 0, 1, \dots)$ . The coupled line filter with arbitrary image admittance and the equivalent circuit is shown in figure3.

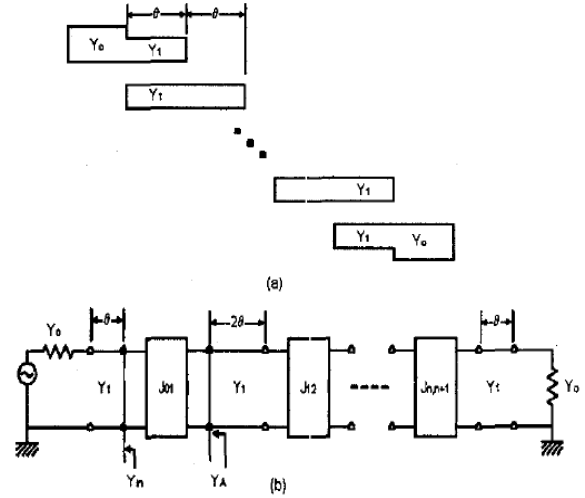


Figure 3. The coupled line filter with arbitrary image admittance  $Y_1$  and the equivalent circuit.

The length, width and spacing of section  $n$ th of the coupling line were represented by  $l_n$ ,  $w_n$  and  $s_n$  respectively. The length of the  $n$ th upper and lower stub segments were expressed by  $l_{s_n}$  and  $l_{s_{n+n+1}}$  respectively.

The initial length of the upper and lower stubs was set to be equal to a quarter of the wavelength. The appropriate initial value of the filter size could be easily determined from the approximate analytical equation [9].

$$\frac{J_{01}}{Y_1} = \frac{J_{n,n+1}}{Y_1} = \sqrt{\frac{\frac{\pi}{2} AW}{\omega' g_0 g_1 - \frac{\pi}{4} AW \left(1 - \frac{1}{A^2}\right)}} \quad (11)$$

$$\frac{J_{12}}{Y_1} = \frac{J_{n-1,n}}{Y_1} = \frac{\pi W}{2\omega_1'} \sqrt{\frac{\frac{1}{2} \left[ \frac{J_{01}^2}{Y_1^2} \left(1 - \frac{1}{A^2}\right) + 2 \right]}{g_1 g_2}} \quad (12)$$

$$\frac{J_{j,j+1}}{Y_1} = \frac{\pi W}{2\omega_1'} \sqrt{\frac{1}{g_j g_{j+1}}}, j = 2, \dots, n-2 \quad (13)$$

where

$$\frac{\omega_1'}{\omega_0} = \frac{\omega - \omega_0}{W \omega_0}, \omega_0 = \frac{\omega_1 + \omega_2}{2} \quad (14)$$

$$W = \frac{\omega_2 - \omega_1}{\omega_0}, A = \frac{Y_1}{Y_0} \quad (15)$$

And  $g_i$  was the element value of low-pass filter prototype.

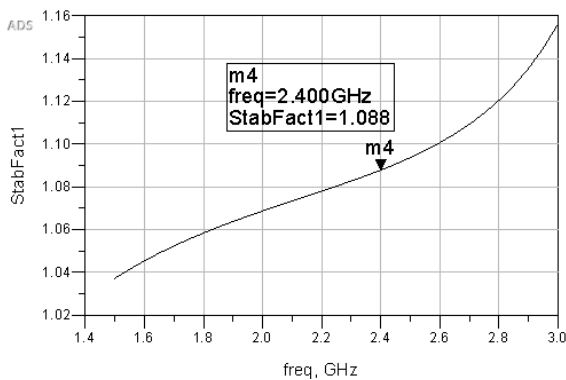
In [10], several methods for reducing phase noise were given:

- (1) The transistor was selected with a lower flicker noise corner frequency  $f_c$ .
- (2) The resonator was selected with a higher unloaded Q value as the frequency selection original.
- (3) The transistor was chosen with a lower noise figure.
- (4) The transistor was try to avoid working in saturation when designing the oscillator.

### 3 Simulation of oscillator

#### 3.1 Simulation of bias circuit

The proper bias point of transistor is set according to transistor datasheet. This paper calculate approximate resistor value and use simulate software ADS to generate bias circuit. And the stability factor  $K$  Should be verified above 1 around centre frequency. In this work,  $K$  is above 1 in the pass band, so there is no need to add feedback inductor on the emmitter of the transistor. And this paper adopt co emitter structure, setting the Bias point a  $V_{ce}=2V, I_c=20mA$ . The bias circuit simulation result is shown in figure4.

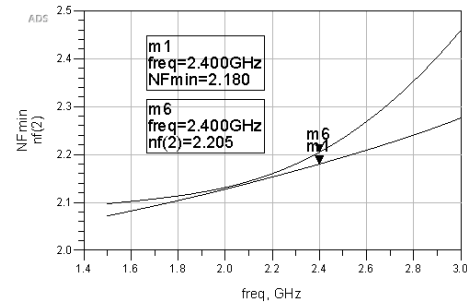


**Figure 4.** Stability factor of bias circuit with frequency weep range from 1.5GHz to 3GHz

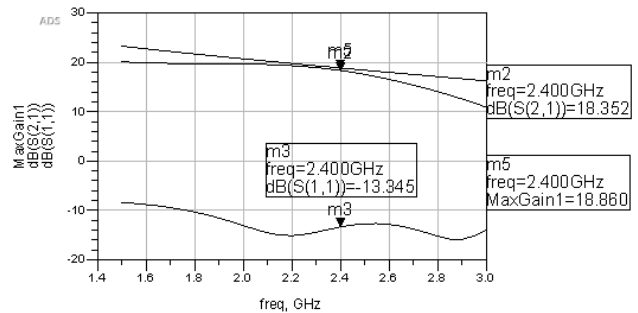
#### 3.2 Simulation of impedance matching

Impedance match on input terminal and output terminal is implemented after the transistor working at proper bias point. There are two ways to implement impedance matching, one is matched by the load to the source impedance; the other is matched by the source impedance to the load impedance. This paper uses the first matching method. In order to reduce the influence of phase noise, the minimum noise matching is used at the input matching end, that is, the impedance value of the system at the minimum noise figure is used as the input impedance of the low noise amplifier. While in order to achieve high output power, the maximum gain matching is used at the output of the low noise amplifier, that is, the impedance value of the theoretical maximum gain at the selected bias point is used as the output impedance, and the load impedance  $50\Omega$  is matched to the conjugate of the output impedance. The impedance matching simulating result is shown in figure 5, in which figure a shows the

comparison of theoretical and actual noise figure and figure b shows the S parameter of the LNA.



a. Comparison of theoretical and actual noise figure

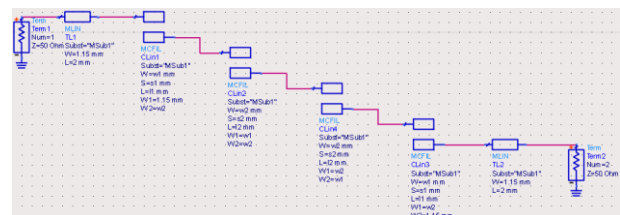


b. S parameter of the LNA simulation

**Figure 5.** Impedance matching result with frequency weep range from 1.5GHz to 3GHz

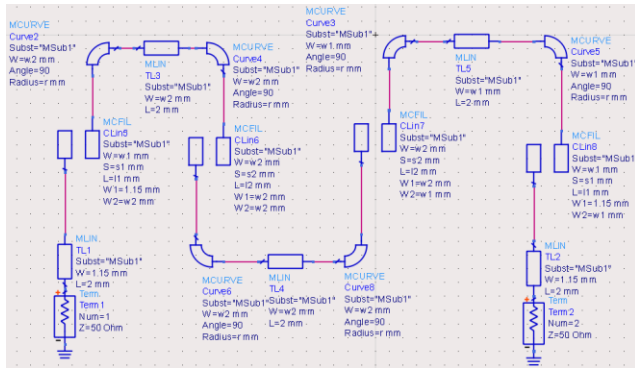
#### 3.3 Simulation of parallel coupled line filter

This paper calculates the approximate length  $l_n$ , width  $w_n$  and spacing  $s_n$  of section  $n$ th of the coupling line, and build low-pass filter prototype module, then create band-pass filter schematic as figure6.



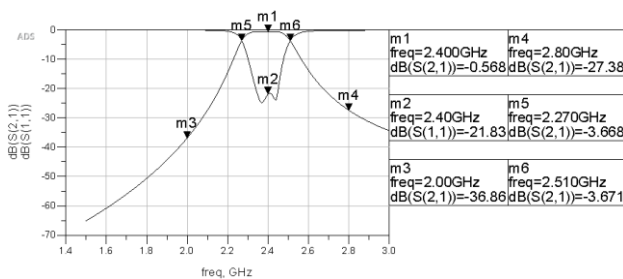
**Figure 6.** Schematic of Parallel coupled micro strip line filter

Considering that the 2.4G wavelength is long, in order to reduce the board size, this paper adjusts the filter to the form of Figure 7. In order to reduce the coupling between the micro strip lines, the micro strip line spacing is adjusted to twice the line width according to experience.



**Figure 7.** Schematic of new form of Parallel coupled filter

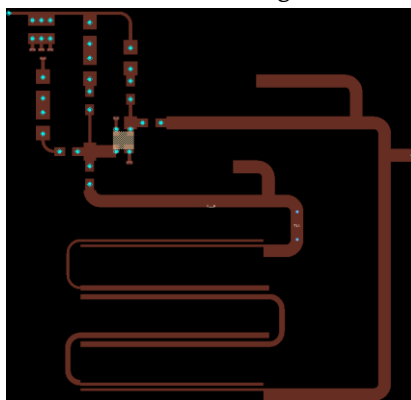
This paper simulates the circuit and optimize the parameters  $l_n$ ,  $w_n$ ,  $s_n$  through the ADS software to obtain the results as shown in Figure 8.



**Figure 8.** S parameter of the filter simulation with frequency sweep range from 1.5GHz to 3GHz

### 3.4 Layout circuit of oscillator

This paper splices the low noise amplifier with the parallel coupled line filter schematic and adjusting the phase line so that the feedback loop phase satisfies an integer multiple of  $2\pi$ . Then generate the layout design of all the schematic as shown in figure9.

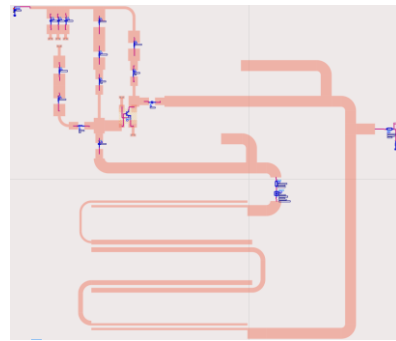


**Figure 9.** Layout of based on a deformed structure parallel coupled line filter oscillator

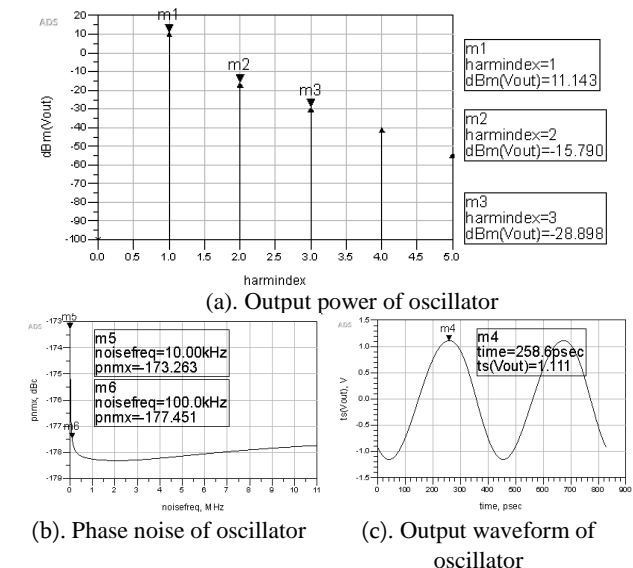
Then this paper implements co-simulation using closed-form electromagnetic and harmonic balance techniques applied to the circuit board and active circuit, respectively.

### 3.5 Results of oscillator simulation

The schematic of co-simulation is shown in figure 10.



**Figure 10.** Schematic of EM and schematic co-simulation  
 The frequency sweep range is set from 1.5GHz to 3GHz. The simulation results are shown in figure 11.



**Figure11.** Results of EM and schematic co-simulation

As the results showed above, the output power is 11dBm, considering machining error. And the phase noise is -173.26 dBc/Hz at 10kHz off centre point, which was better than -88 dBc/Hz in [1]; and the phase noise was -177.45dBc/Hz, which was better than -102 dBc/Hz in [6] and -103dBc/Hz in [10] with the use of substrate integrated waveguide(SIW).

The results meet design requirements, with a standard sine wave outputting.

## 4 Conclusion

This paper proposed an oscillator based on a deformed structure parallel coupled line filter design, and the size of the circuit board was 40mm\*40mm. The design results meet the design specifications and leave a margin.

This design can be used in designs such as through-wall radars that require high output power and low phase noise.

Moreover, this design can be used to add other functions such as phase-locked loop integrated circuits according to different needs. It is also possible to reduce the size of the frequency selection circuit by using a substrate integrated waveguide(SIW) structure with a higher Q value.

## Acknowledgment

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