Design Issues for NEM-Relay-Based SRAM Devices

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Abstract. We analyze the design constraints of six transistor SRAM cells that arise when using nanoelectromechanical relays. Comparisons are performed between a CMOS 6T conventional SRAM cell and various hybrid memory cells built by replacing a selection of MOSFET transistors with NEM relays. Impact on important memory cell parameters such as various reliability metrics like static noise margin and write noise margin and power consumption are evaluated from circuit simulations using a Verilog-A compact model of the nanomechanical relay. We found that the use of relays involve a new challenge in the design of SRAM hybrid devices as the readability and writeability of the resulting cells manifests a strong dependence with the value of the contact resistance of the NEM relay, a parameter that can experience important variations with the continued operation of the device.

1 Introduction

SRAM has been the predominant module used to implement storage in integrated circuits [1]. Dense and fast on-chip memories are essential to increase the computational power and speed of modern systems on chip (SOC). However, as a consequence of scaling, memory blocks implemented with the conventional six transistors cell (6T-cell) become more sensitive to device variations, and more prone to functional failures than before. In addition, their power consumption in stand-by has increased notably due to the increase of transistor OFF-state leakage currents and memory size [2].

Despite these facts, SRAM cells must stand stable during read and writeable during write. Cell stability during read is improved by strengthening the internal latch inverters and weakening the access transistors, while the opposite is desired for cell write-ability, imposing conflicting constraints on transistor sizing of 6T-cells [3]. To ensure adequate *read*/*write* margins, SRAMs must be operated above a minimum supply voltage in *hold* mode, blocking the possibility of reducing stand-by power consumption related to leakage currents. Since leakage power is proportional to the transistor number, and given the large memory content of present SOC devices, it becomes a relevant issue at the point that the increase of leakage current is hindering the implementation of energy-efficient designs.

The advancements in the development of surface micromachining processes for micro and nano-electro-mechanical systems (MEMS/NEMS) during these last years, has revivified the idea of using mechanical switches to implement digital logic circuits. Nano-electromechanical (NEM) relays are one interesting class of emerging devices that shows a subthreshold behaviour similar to an ideal switch (Fig. 1). Recent works have demonstrated that NEM relays could be manufactured reliably and used to build complex-integrated logic circuits [4,5]. Chong et al. [6] suggested the use of NEM relays, to overcome some of the inherent limitations of conventional CMOS 6T SRAM cells.

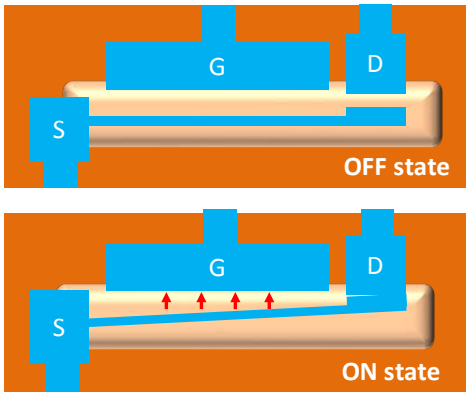

Fig. 1. Illustration of an electrostatic 3T relay (Top view). (up) Relay in OFF state. (down) Relay in ON state due to application of an electrostatic force between Gate and Source terminals.

Compared with MOS transistors, an electrostatically driven relay offers many advantages:

- Significant reduction in standby power consumption. Leakage current is negligible due to the physical gap distance between the two electrodes in the OFF state.
- Abrupt switching behaviour, with subtreshold Swing ≈ 0, which enables very small operating voltage swing (determined by the hysteresis voltage) [7].

These two advantages make NEM-relay-based circuits potentially more energy efficient than their CMOS counterparts [8,9]. To avoid performance limitations of the relatively long mechanical delay of the

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NEM relays, co-integration of NEM relays and CMOS transistors is the most promising solution to achieve a good balance of energy efficiency and information processing throughput. In this paper we will explore the new circuit constraints related to their use in the design of hybrid SRAM memories.

2 MOSFET vs relay

Relays use the mechanical motion of a movable electrode (beam or membrane) to make/break physical contact between two electrically conductive nodes to switch current *ON/OFF*. Nano-electromechanical relays are essentially three or four terminal mechanical switches that are electrostatically actuated.

Devices with a minimum of three terminals (one control and two outputs) are required for a logic relay. Fig. 1 shows a three terminal electrostatically actuated NEM relay (3T-NEMR), which consists of: a gate (G), a source (S), and a drain (D). The 3T-NEMR operate similarly to field effect transistors: when the electrostatic force is strong enough to overcome the spring–mass–damper mechanical system, the suspended cantilever connects source and drain and turns the switch *ON*. At this point a current at contact will flow between the two nodes, whose value will be determined by the contact resistance (R_C). When the switch is *OFF*, the source is mechanically disconnected from the drain and hence the leakage through the device is zero (in fact at nanometer scale this current is limited to vacuum tunnelling and Brownian motion displacement currents, that appear in the physical gap that separates the mobile structure and the electrode) [10].

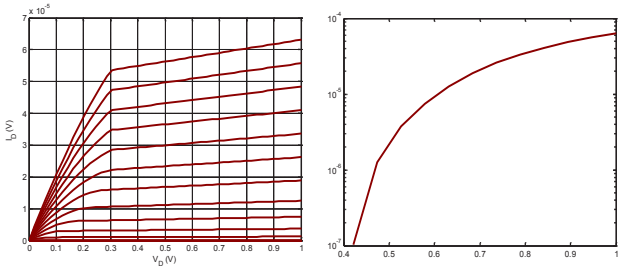

Fig. 2. MOSFET I_{DS}-V_{DS} and I_{DS}-V_{GS}.

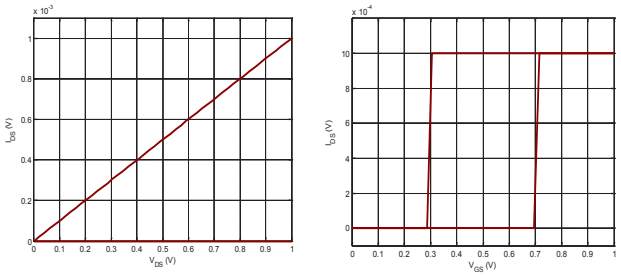

Fig. 3. I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristic of the 3T-NEMR.

As in MOSFETS, the current flow between the source and the drain is controlled by the gate bias voltage. However, there are important differences: (i) they have zero off-state leakage. (ii) They have a sharp on/off transition. (iii) The turn-on voltage is larger than the turn-off voltage (hysteresis). (iv) the I_{DS} current does not depend on V_{GS}. Figs 2 and 3 compare the *I-V* characteristics of MOSFET and 3T-NEMR devices.

The mechanical delay, τ_{mech}, is the time it takes for the beam to move from the non-deflected state to the state of contact with the drain electrode, it must be low enough to ensure that it does not become the time-limiting factor in circuit operation [6].

Adding a fourth "body" electrode will allow decoupling control and signal to implement true pass gates. An example of a 4-Terminal electrostatic switch with insulated channel attached to the movable electrode [11] is shown in Fig. 4. The fabrication of this device is more challenging [12], and less trivial to implement with standard CMOS technology.

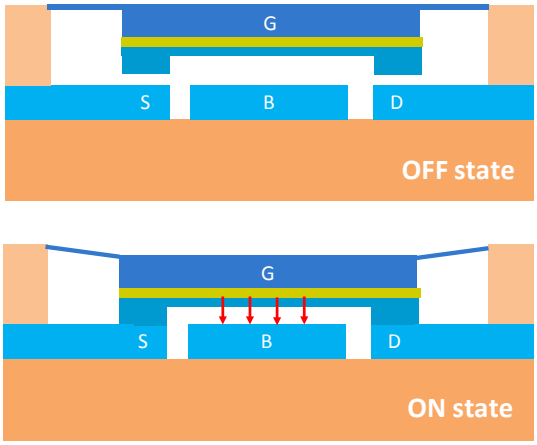

Fig. 4. Illustration of an electrostatic 4T relay based on a suspended membrane (Cross section). (up) *OFF* state. (down) *ON* state (produced by the application of an electrostatic force).

3 3T-NEMR design

Fig. 5 shows a top view of the 3T relay, consisting of a thin cantilever implemented with one of the metal levels available in standard CMOS technologies. The gate is electrostatically actuated whenever there is a voltage higher than a pull-in threshold voltage, V_{pi}, between the gate and source. When the NEMR is in its *ON*-state and voltage V_{GS} is lowered, the electrostatic force reduces and eventually will open the relay once it crosses a pull-out threshold voltage V_{po}. Usually the pull-out voltage is lower than the pull-in voltage due to the reduction of the gap distance and the possible presence of adhesion forces [13].

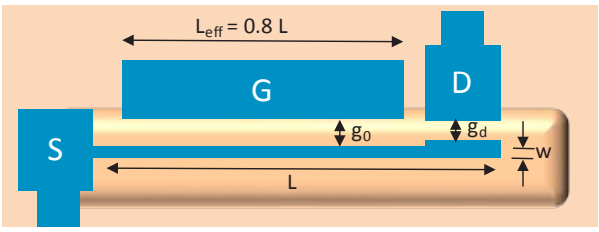

Fig. 5. 3T-NEMR top view (geometrical parameter definition)

3.1 Geometrical parameters

The geometrical parameters of the cantilever are usually determined by the designer with the aim to operate with

the nominal voltage of a given CMOS technology. The voltage required to turn *ON* the relay is given by [14]:

$$V_{pi} = \sqrt{\frac{8\,k\,g_0^3}{27\,\varepsilon_0\,A_{ov}}} \quad (1)$$

ε_0 is the permittivity of free space, A_{ov} is the area of overlap between gate and source electrodes ($A_{ov}= t\times L_{eff}$, t is the cantilever thickness and L_{eff} the effective length), g_{off} is the gap between electrodes when switch is *OFF* and k the effective spring constant (stiffness) given by:

$$k = 16\frac{E\,t\,w^3}{L^3} \quad (2)$$

where E is the cantilever Young modulus. Taking into account that E and t are set by the technology, w and g_{off} are limited by DRC rules (note from Eq. (1) and (2), that these parameters must be as low as possible to minimize V_{pi}), it follows that cantilever length is the only available design parameter to set the pull-in voltage.

3.2 Contact Resistance

The quality of the electrical contact between source and drain is determined by their contact resistance R_c. The notion of contact resistance is not as trivial as it may first appear. It involves the physics of contact mechanics with electrical conduction. Due to roughness of the contacting surfaces, only some small parts within the apparent contact area are in physical contact when the relay is in the *ON* state. In addition, some of those contact points might not be conductive. In a NEM relay, the contact resistance, R_c, can be determined using the Sharvin model [15],

$$R_c = 4\rho\ell/3\pi r^2 \quad (3)$$

Where ρ is the electrical resistivity, ℓ represents the electron mean free path, and r the radius of the contacting asperity. In practice, values of contact resistances of several kΩ are allowed since the digital circuit operating speed is limited by the mechanical switching delay of the relay rather than the electrical delay related to RC product [16].

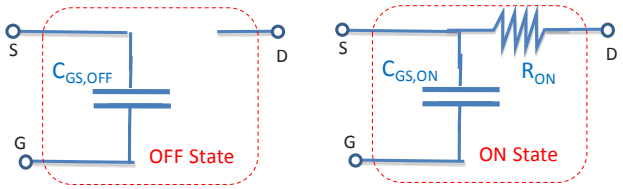

Fig. 6. Electrical model of the 3T-NEMR.

3.3 Verilog-A model

To perform electrical analysis of circuits containing mechanical switches, we developed a Verilog-A model for the 3T-NEMR based on [6] (Fig. 6). The model describes the following behavior:

- Current between source and drain is zero when the relay is in its *OFF*-state.
- The relay turns from *OFF* to *ON* with a delay τ_{mech} when V_{GS} rises over the pull-in voltage V_{Pi}.
- The relay switch to *OFF* when the device is in its *ON* state and V_{GS} decreases below V_{po}. Due to the difference in distance that must be traveled to break the contact between drain and source, the delay needed to switch from *ON* to *OFF* is considerably lower than τ_{mech} [7].

The model is based in the following electrical parameters:

- The contact resistance, R_c, as commented, is the resistance between source and drain when the device is in its *ON*-state. It must be measured experimentally.
- $C_{GS,OFF}$, the capacitance between source and gate in *OFF* mode. It is computed by:

$$C_{GS,off} = \varepsilon_0\times t\times L_{eff}/g_{off} \quad (4)$$

- $C_{GS,ON}$, the capacitance between source and gate in *ON*. g_{on} corresponds to the new average gap distance as a consequence of the beam movement.

$$C_{GS,on} = \varepsilon_0\times t\times L_{eff}/g_{on} \quad (5)$$

- The mechanical delay, τ_{mech}, given by [17]

$$\tau_{mech} = 3.67\sqrt{\frac{M}{k}} \quad (6)$$

Where M is the cantilever effective mass

$$M = 0.2427\,\rho_m\,w\,L\,t \quad (7)$$

being ρ_m, the metal density.

- The pull-in voltage, V_{pi}, given by Eq. (1).
- The pull-out voltage, V_{po}, obtained as:

$$V_{po} = \sqrt{\frac{2k\left(g_{off}-g_{on}\right)g_{on}^2}{\varepsilon\,t\,L_{eff}}} \quad (8)$$

4 NEMS based SRAM

Fig. 7 represents the basic schematic of the conventional six transistors SRAM cell. In CMOS technology, pull-down devices PD_1, PD_2 and pass transistors PT_1 and PT_2 are nMOS transistors while pull-up devices PU_1 and PU_2 are pMOS transistors.

Due to the switching behavior of NEM relays shown in Fig. 3, conventional MOSFET transistors can be substituted by NEM switches. nMOS pull-down devices can be replaced by 3T-NEMR with their source terminal connected to *gnd*. pMOS pull-up devices can be replaced by a similar 3T-NEMR with their source connected to V_{DD}. A more challenging 4-terminal relay like the one presented in [11] is needed to replace the access gate. According to this, we have analyzed the configurations reported in Table 1. In order to assure a similar behavior from 1-to-0 and 0-to-1 transitions, only symmetrical configurations have been considered.

To face the design of these cells, we must bear in mind the two imperative functional constraints related to SRAM design in any advanced technology:

i. The cell must be able to retain data during *hold* and *read*.
ii. The cell must be able to change its content from 0 to 1 or from 1 to 0 during *write*.

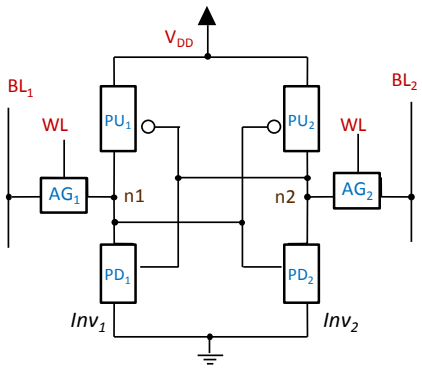

Fig. 7. SRAM cell.

TABLE 1. SRAM configurations

	PD1	PD2	PU1	PU2	PT1	PT2
6T	nMOS	nMOS	pMOS	pMOS	nMOS	nMOS
6N	3T NEMR	3T NEMR	3T NEMR	3T NEMR	4T NEMR	4T NEMR
4N	3T NEMR	3T NEMR	3T NEMR	3T NEMR	nMOS	nMOS
2NU	nMOS	nMOS	3T NEMR	3T NEMR	nMOS	nMOS
2ND	3T NEMR	3T NEMR	pMOS	pMOS	nMOS	nMOS

In conventional 6T designs, both constraints are usually achieved by appropriate selection of the drive-strength of each transistor, a feature that is proportional to the transistor width. W_n denotes the width of transistors PD_1 and PD_2, W_{acc} is the width of the access transistors AG_1 and AG_2, W_p corresponds to the width of PU_1 and PU_2. In a read operation (usually performed with both bit-lines precharged to '1'), the access transistor disturbs the "0" storage node by pulling it up, assuming the cell in initial state (V_{n1}=0, V_{n2}=V_{DD}), the voltage at node n_1 increases to a positive value V_{READ}. If V_{READ} becomes higher than the trip point V_{TRIP} of the inverter INV_2, then the cell flips while being read. Typically, to guarantee a non-destructive read with an adequate tolerance level, the cell ratio, defined as $CR=W_n/W_{acc}$, is usually comprised between 1.5 and 3 [18] (CR can also be regarded as a drive-strength ratio).
A write failure occurs when a pass transistor is not strong enough to overpower the pull-up pMOS transistor. The requirement to perform a write operation is typically met by setting an adequate pull-up ratio ($PR= W_p/W_{acc}$) usually lower than 2. According to this, to minimize cell area, the size of the pull-up and pass transistors are typically chosen to be minimal $W_p=W_{acc}=W_{min}$ $(PR=1)$ [18], while W_n is set to a value close to $2\times W_{min}$ to guarantee a non-destructive read.

The scenario changes drastically when using NEM relays, as in practice we do not have any design parameters to control the drive-strength of these devices. In fact, it depends on R_c, which in principle is a technological parameter. Therefore, a correct analysis of the influence of this parameter in cell behavior will be essential to assure the functional behavior of cells implemented with relays. The different configurations in Table 1 are analyzed in the following subsections.

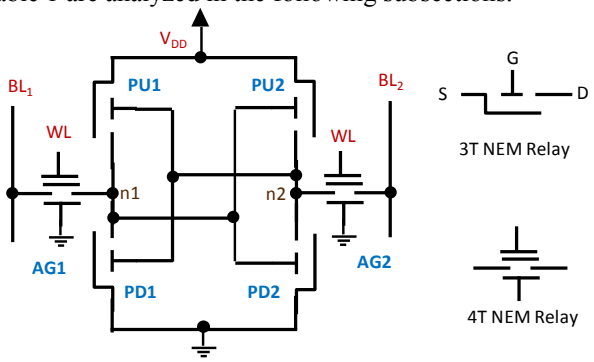

Fig. 8. 6N NEMR SRAM bit-cell.

4.1 NEMR based bit-cell (6N)

Fig. 8 represents the schematic of the only-NEMR based bit-cell formed by four 3T-NEMR and two 4T-NEMR. R_{3T} represents the contact resistance of the 3T-NEMR, while R_{4T} is the contact resistance of the 4T-NEMR devices (access gates). If we set the initial condition as $V_{n1}=0$, $V_{n2}=V_{DD}$ (the other possible initial condition, $V_{n1}=V_{DD}$, $V_{n2}=0$, would lead to identical results), to assure that the bit-cell logic state is retained during a read access, it must be verified that the increase in voltage V_{n1} induced by the read access, is not high enough to switch inverter PU_2-PD_2, which is equivalent to saying that conditions $V_{n1}>V_{pi}$ and $V_{n1}>(V_{DD}-V_{po})$ are not both satisfied. We define $V_{max,r}=max[V_{pi}, (V_{DD}-V_{po})]$, then it follows that:

$$R_{c,PD} \le \frac{1}{\frac{V_{DD}}{V_{\max,r}}-1} R_{cx} \tag{9}$$

On the other hand, we must be able to modify the logic state of the cell by means of a write access. During *write*, the node that is at V_{DD}, must decrease enough to switch the inverter PU_1-PD_1 (Eq. 9 prevents the node at 0 V from rising enough to start the process), which is equivalent to say that conditions $V_{n1}<V_{po}$ and $V_{n1}<(V_{DD}-V_{pi})$ are not both satisfied. We define $V_{min,w}=min[V_{po}, (V_{DD}-V_{pi})]$, then it follows that:

$$R_{c,PD} \ge \left(\frac{V_{DD}}{V_{\min,w}}-1\right) R_{cx} \tag{10}$$

When all 3T-NEMR devices are similar, it turns out that $R_{c,PU}=R_{c,PD}=R_c$. Taking into account that $V_{min,w}+V_{max,r}=V_{DD}$, we get to the result that there is only a possible resistance value that satisfy both conditions.

$$R_c = \frac{1}{\frac{V_{DD}}{V_{\max,r}}-1} R_{cx} \tag{11}$$

It results a bit-cell with serious functional problems. To elude them, two different 3T-NEMR devices with different contact resistance (or different V_{po}, V_{pi} values) would be required.

4.2 4N bit-cell

In this configuration, only the four transistors forming the internal latch are substituted by 3T-NEMR devices. Again, the condition $V_{n1}<V_{max,r}$ is required to assure logic state retention during *read*. The V_{n1} value can be obtained by applying KCL at node n_1, as PU_1 is *OFF*, $I_{DS,AG1}=I_{PD1}$. Assuming that transistor AG_1 is saturated for V_{n1} values close to $V_{max,r}$, it results:

$$R_{c,PD} \le \frac{2V_{\max}}{\beta_x \left(V_{DD} - V_{\max} - V_{T,x}\right)^2} \quad (12)$$

Where β_x and $V_{T,x}$ are the transconductance and threshold voltage of the AG_1 transistor (the unified transistor model in fig. 9, proposed in [19] has been used in the analysis). Given the values of the involved parameters, Eq. 12 is fulfilled even for relatively large values of $R_{c,PD}$ (> 100 KΩ). In fact, the condition is met for any resistance value when $V_{pi}>(V_{DD} - V_{T,x})$.

$$\begin{cases} I_D = 0 & V_{GT} \le 0 \\ I_D = k\frac{W}{L}\left(V_{GT}V_{\min} - \frac{V_{\min}^2}{2}\right)\times\left(1+\lambda\cdot V_{DS}\right) & V_{GT} \ge 0 \end{cases}$$

$$V_{GT} = V_{GS} - V_T$$

$$V_{\min} = \min(V_{GT}, V_{DS}, V_{DSAT})$$

$$V_{DSAT} = L\frac{v_{sat}}{\mu}$$

Fig. 9 Unified transistor model form [19].

Cell writing is possible when the internal node being high (node n_2 according to our initial conditions) is capable to fall below $V_{min,w}$ when connected to a bit-line at 0 V through the access gate. As PD_2 is *OFF*, the V_{n2} value can be obtained by applying KCL at node n_2: $I_{DS,AG2}=I_{PU2}$. Assuming that transistor AG_2 is in velocity saturation region for V_{n2} values close to $V_{min,w}$, it results:

$$R_{c,PU} \ge \frac{V_{DD} - V_{\min}}{\beta_x \left(\left(V_{DD} - V_{T,x}\right)V_{Dsat} - \frac{{V_{Dsat}}^2}{2}\right)} \quad (13)$$

Both conditions can be satisfied, however, since they depend on technological parameters, care should be taken when using this topology.

4.3 2NU bit-cell

Only the pMOS pull-up devices are replaced by 3T-NEMR. Read stability depends on the cell-ratio as in the conventional 6T bit-cell, we consider that we will not have problems on this side when maintaining 6T cell ratio. In addition, we will even have some extra margin since the voltage level needed to switch the NEMR at PU_2 is even greater than the trip voltage of the CMOS inverter in the 6T bit-cell.

A condition similar to Eq. 12 can be derived to assure cell-writing. It is only necessary to replace $V_{min,w}$ by $(V_{DD} - V_{pi})$ as a NEMR is not used to implement the PD device.

$$R_{c,PU} \ge \frac{V_{pi}}{\beta_x \left(\left(V_{DD} - V_{T,x}\right)V_{Dsat} - \frac{{V_{Dsat}}^2}{2}\right)} \quad (14)$$

Similar precautions than in the previous case must be taken.

4.4 2ND bit-cell

Only the nMOS pull-down devices are replaced by 3T-NEMR. The condition to assure logic state retention during a read access is now $V_{n1}<V_{pi}$. As PU_1 is *OFF*, voltage V_{n1} can be obtained by applying KCL at node n_1: $I_{DS,AG1}=I_{PD1}$. Assuming that transistor AG_1 is saturated for V_{n1} values close to V_{pi}, it holds:

$$R_{c,PD} \le \frac{2V_{pi}}{\beta_x \left(V_{DD} - V_{pi} - V_{T,x}\right)^2} \quad (15)$$

As commented before, this condition is satisfied for any contact resistance when $V_{pi} > V_{DD}-V_{T,x}$, alternatively it will allow relatively large values on R_c.

Cell-writeability is not a concern in this configuration, as it depends on the strength ratio between the pMOS Pull-Up transistor and the nMOS access-gate as in the 6T bit-cell. Voltage at node n_2 must decrease below V_{po}, a condition usually meet for pull-up rations close to 1 (except for very low values of V_{po}).

5 Results and discusion

The transient behavior of the cells during *read* and *write* has been simulated with Spectre using the Verilog-A model described in section 3, and transistor models of a commercial 65 nm CMOS technology. Table 2 lists the geometrical and electrical parameters of the Verilog-A model, computed with Eqs. (1)-(8).

TABLE 2. NEMR PARAMETERS

w (nm)	**t** (nm)	**L** (nm)	**g_0** (nm)	**k** (N/m)	**M** (kg)
50	200	3	20	1.7	6.52e-17

V_{po} (V)	**V_{Pi}** (V)	**$C_{GS,ON}$** (fF)	**$C_{GS,OFF}$** (fF)	**τ_{mech}** (ns)
0.69	0.98	0.21	0.64	22

As expected from the previous analysis, we have observed that the 4N bit-cell does not show any problem during *read* for contact resistances in the range of values comprised between 1KΩ and 1MΩ, although it becomes non-writeable for R_c values lower than 5.8 KΩ (Fig. 10), this behavior is in concordance with Eq. 13. According to Eq. 13, to change the state of the bit-cell during *write*,

R_c must be greater enough (some KΩ). The values of V_{sat}, V_T and β_x in Fig. 9, have been fitted from the I_D-V_{DS} characteristics obtained from the transistor models provided by the foundry.

A similar behavior have been observed in 2NU cells (Fig. 11), the cell becomes non-writeable for R_c values lower than 6.4 KΩ, a result that is qualitatively described by Eq. (14). Finally, in Fig. 12, we present simulation results corresponding to the 2ND cell. For simplicity, we only present results from a low value (1 KΩ), and a high value (1 MΩ) of R_c. Note that both *read* and *write* operations can be performed satisfactorily in concordance with our analysis.

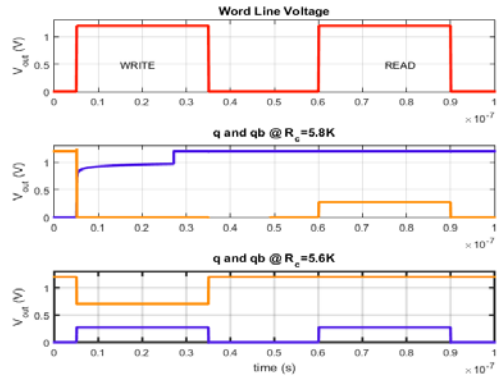

Fig. 10. *Write* and *Read* operation in a 4N bit-cell. *Write* fails por R_c values lower than 5.8 KΩ (assuming a minimum size pass-transistor).

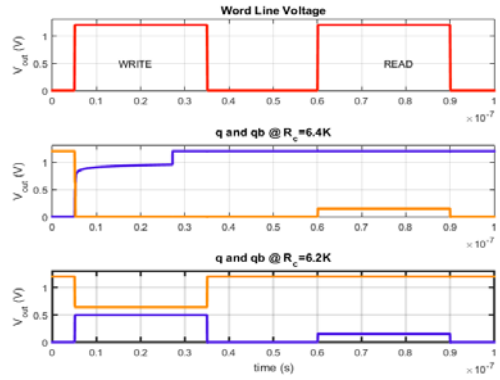

Fig. 11 *Write* and *Read* operation in a 2NU bit-cell. Write fails por R_c lower than 6.4 KΩ (assuming a minimum size pass-transistor and *CR*=2).

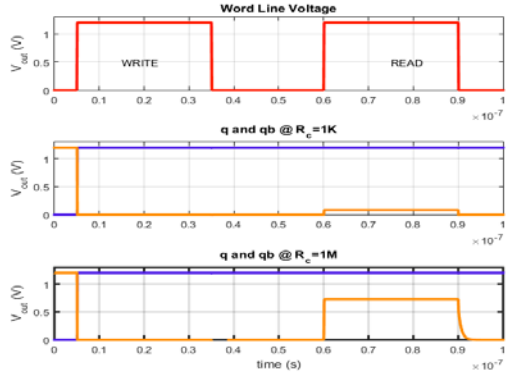

Fig. 12 *Write* and *Read* operation in a 2ND bit-cell (assuming minimum size pull-up and pass-transistor).

From the analysis we have shown that the contact resistance is an important technological parameter for NEM relays. Its value is difficult to control as it involves the physics of contact mechanics with electrical conduction. This will imply a challenge in the design of SRAM devices based on NEM relays as the readability and writeability of the resulting cells is determined by the value of contact resistance.

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