Analysis of Anti-JFET for 600V VDMOS and HCI Reliability

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Abstract. In VDMOS device the anti-JFET concentration has important role for determining the breakdown voltage and on-resistance of the device. Because higher N-drift doping concentration can provide the very best on-resistance of the device but also decrease breakdown voltage. It also has a proportional relationship with threshold voltage degradation. In this paper, we report the anti-JFET implantation energy influence effect electric potential distribution, the highest impact ionization shifted from the silicon surface to deeper. It will have less hot carrier impact, and we have found higher breakdown voltage. The anti-JFET implantation is critical for on-resistance off-state breakdown voltage optimization, However the high field and high impact ionization near the gate region will cause severe hot carrier Injection problem. The general expectation of high voltage VDMOS transistor is to have higher breakdown voltage, less degradation due to hot carrier injection and better on-resistance.

1 Introduction

This device structure is fabricated by starting with an N-type epitaxial layer grown on a heavily doped N type substrate. The channel is formed by the difference in lateral extension of the P-base and N type source regions produced by their diffusion cycles. Without the application of a gate bias, a high voltage can be supported by the VDMOS structure when a positive bias is applied to the drain. The general VDMOS device has high breakdown voltage, lower on-resistance and less hot carrier impact. In this study objective of reducing the efficiency of the junction field effect transistor by mean of introducing an anti-JFEF implant in the fabrication process.

The present work is a continuation of that described in, with the objective of reducing the efficiency of the junction field effect transistor by mean of introducing an anti-JFE implant in the fabrication process. The optimization of the implanted dose leading to the optimum trade-off between the on-state resistance and the breakdown voltage.

The contribution of the Junction Field Effect Transistor resistance R_{JFET} , the resistance of the region between the p-base diffusions, depends on the spacing and depth of the p-base diffusions and the doping concentration of the drift region.

The resistance of the epi layer R_{Epi} is dependent on its doping concentration and its thickness. Its value can be lowered by increasing the doping concentration or by decreasing the thickness of the epi layer. The resistance

of the epitaxial layer dominates R_{on} for high voltage devices.

Fig. 1. Net doping profile of the anti-JFET region $3.5E12$ at 360keV implanted.

This article summarizes the TCAD and experimental results of this technique when applied for the improvement of device stability and lifetime.

2 Simulation methodology

The simulations are done by using Synopsys software. The VDMOS transistor device is virtually fabricated using tsuprem4 and characteristics are simulated by using Medici. In this paper, we work done by varying the doping concentration and energy of anti-JFET region,

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and study the result based on the threshold voltage degradation caused by hot carrier injection. In order to optimize the dose and energy of the anti-JFET implant. The difference distribution of electric potential in line with anti-JFET implanted dose (a) high dose ($3.5E12$) (b) low dose ($1.5E12$) at 360keV as shown Fig.2.

These simulations show a reduction of the on-state resistance 15.4% and breakdown voltage only losing 4.75% at energy 360keV. For VDMOS transistor a high equipotential under the gate is the major reason of the device. In this paper, we simulated portion of the VDMOS transistor for the JFET implant of dosage and energy variation. The anti-JFET implanted dose trade-off between the breakdown voltage and on-resistance as shown Fig.3. The on-state resistance of the VDMOS transistor can be significantly reduced by introducing a blanket anti-JFET implant without a major impact on the voltage capability.

Fig. 2. The equipotential lines have lower and also had better HCI reliability. (a) High dose (b) Low dose

Fig. 3. Variation of off-state breakdown voltage and on-state resistance with anti-JFET implant process.

Fig. 4. The VDMOS transistor with anti-JFET energy 360keV measured up to stress $1E4$ seconds and after that we have measured V_{th} degradation of the device.

Carriers generated by impact ionization can themselves gain enough energy (call hot carriers) to be injected into the gate oxide. We observed if equipotential line crowding then HCI reliability is worse. In this paper, thermodynamic HCI were invoked in the device simulation to perform the interface trap generation due to HCI. For VDMOS transistor a high field under the gate region is the major source of the device degradation.

Hot carrier stress experiments were performed under $V_{gs}=5V$ and $V_{DD}=600V$, the simulation of reliability based on anti-JFET implantation energy at 360keV. On the other hand, electron injection and trapping at the SiO_2/Si interface in the gate oxide and the major cause of the degradation of threshold voltage which increases constantly throughout stress time as shown Fig.4.

We found threshold voltage degradation reduced 37.5% from $3.5E12$ to $1.5E12$ at $1E4$ stress times.

Fig. 5. The device lifetime curve between V_{th} and stress time

We have stressed this cool device for almost 11 years and found as shown in Fig.5. Only a small amount of ΔV_{th} after 1 year is observed throughout the rest of stress time. Assuming donor and acceptor traps (pre-existing prior to stress) at the JFET field region (near to the channel), V_{th} increases with electron injection (or trapping at the acceptor states), and it finally starts to decrease by new donor type interface traps, which correspond that the negative charge by electron injection is compensated by the positive charge build-up at the Si/SiO_2 interface and in the oxide.

(a)

Fig. 6. Trapped charge distribution of the anti-JFET 1.5E12 at 360keV implanted after (a) 0 second (b) 3.5E8 seconds of HCI stress.

In this reliability test, we can observe that trapped charge distribution after HCI stress 0 second and 3.5E8 seconds. From Fig.6 the trapped charge in the order of 1.658×10^{16} but after 3.5E8 seconds HCI stress time it is in the order of 8.257×10^{16} . It is approximately 5 times more traps for 0 second compared to 3.5E8 seconds.

3 Conclusion

The paper proposed vertical DMOSFET transistor, the JFET doping concentration has a relation with the threshold voltage degradation. The effects of anti-JFET implant on the on-resistance, blocking capability and the reliability of the VDMOS have been studied. Experimental results show that the anti-JFET implant can reduce the threshold voltage degradation by moving higher field region to the surface channel region. It's highly influence the breakdown voltage and on-state resistance, and less hot carrier induced device degradation. Optimized dose and energy, improve the trade-off between the breakdown voltage and on-state resistance with a good device lifetime.

From our experiments we proved the device after 10 years stress, the breakdown voltage still holds. Therefore, this device has very good HCI performance.

Acknowledgment: The authors would also like to thank National Center for High-performance computing, National Nano Device Laboratories, and the National Chip Implementation Center for supporting us.

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