Comparison of bulk FinFET and SOI FinFET

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Abstract. In this study, we compare the differences and advantages between Bulk FinFET and SOI FinFET. The results are simulated by using the ISE TCAD software. By changing the parameters of the gate voltage, drain voltage and gate length to analysis which characteristic is better. Through the experiment results, we demonstrate that the SOI FinFET have the better characteristics than bulk FinFET[1].

1.INTRODUCTION

With the rapid development of technology, the device structure is very important. The main difference between the Bulk and SOI process is the different substrate, resulting in different process levels. A single-crystal silicon process have used on the SOI FinFET that the device must be deposited on the oxide layer is more difficult to control and the SOI Wafer is relatively more expensive; however, the bulk FinFET is difficult to control the values of parameters because of channel impurities[2]. The bulk FinFET has fewer steps of process and lower manufacturing costs. But, the process consumes high power and large leakage current ; SOI FinFET have the additional layer of oxide (BOX), the difference between the elements can be shortened by removing the n-well or p-well, and the BOX insulation reduces the device leakage[3]. As the results, in terms of the electrical simulation, SOI FinFET is better than Bulk FinFET.

2.Device Structure and Fabrication

The BULK FinFET consists of a diode and two adjacent PN junctions shown in Figure 1 (a), which is the most important circuit component in an integrated circuit with less process steps, lower manufacturing costs, and lower process costs high power, large leakage current. However, the SOI FinFET has more Buried Oxide (BOX) than the BULK FinFET shown in Figure 1 (b), the BOX insulation effect reduces the component leakage and consumes less power in the manufacturing process, but the manufacturing cost is higher.

Figure 1. (a) It is the structure of BULK FinFET.(b) It is the structure of SOI FinFET.

3.Results

3.1 $I_D - V_G$ Characteristic diagram

In the simulation of $I_D - V_G$ characteristic curve shown in Figure 2, we choose different drain operating bias under the conditions of channel length (L_g) of 10um. We hope to observe that the current of BULK FinFET and SOI FinFET is on (I_{on}) and off (I_{off}) between the changes and observe the different curves of the swing and displacement to understand its characteristics. From the $I_D - V_G$ characteristic curve, it can be seen that when the drain bias is large, the circulating current is larger, the ratio I_{on} and I_{off} Ratio will be larger, and the sub-critical swing (SS) will be smaller. On the one hand, SOI FinFET also has better switching efficiency than BULK FinFET.

Figure 2. We can observe that the threshold swing (SS) characteristic of SOI FinFET is better than BULK FinFET.

3.2 $I_D - V_D$ Characteristic Diagram

It can be observed from Figure 3 (a) (b) that the electrical diagrams of the curves of the SOI FinFET and BULK FinFET at different voltages are shown in Figure 3. It can be clearly observed that the current of SOI FinFET is almost saturated at $V_D = 1$ V. It is higher than the saturation current of BULK FinFET shown in Figure 3 (c).

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Figure 3. (a)(b) we can observe the characteristic of current when V_G is 1v, 2v and 3v.(c) When both components reach saturation current, it can be seen that the saturation current of SOI is larger than BULK.

3.3 Electronic Concentration Chart

Due to the experimental simulation I chose NMOS, and I capture the cross-section of the channel to observe the conduction of electrons turning on in the channel. When the channels of SOI FinFET and BULK FinFET are on, it can be observed from Figure 4(a) that the concentration of SOI FinFET is higher than BULK FinFET. In addition, the leakage current of BULK FinFET is more severe than SOI FinFET. However, when the channels of SOI FinFET and BULK FinFET are off, it can be observed from Figure 4(b) that the concentration of SOI FinFET is greater than BULK FinFET. Although BULK FinFETs are well-closed, the electron concentrations SOI FinFETs is higher than BULK FinFETs.

Figure 4. We can observe the electron density in SOI FinFET when(a) I_{ON} and(c) I_{OFF} . On the other hand, we show the electron density in BULK FinFET when(b) I_{ON} and(d) I_{OFF} .

3.4 $I_D - V_G$ Characteristic Diagram (DIBL value)

When the off-state transistor has a high drain voltage, making the barrier between the source and the channel down, it results a nearly through phenomenon called DIBL (Reduced Induced Drain Barrier). Figure 5 shows that when I_D is fixed, there is no difference between $V_G = 1$ and $V_D = 0.05$ for the SOI FinFET shown in Figure 5 (a), but the difference between the $K = 1$ and $V_D = 0.05$ for the BULK FinFET varies greatly shown in Figure 5 (b). From this it can be found that DIBL of BULK FinFETs have more severe than SOI FinFETs.

Figure 5. The $I_D - V_G$ characterization of SOI FinFET(a) is better than Bulk FinFET(b).

3.5 DIBL - L_G characteristic diagram

It can be observed from Figure 6 that as the channel length (L_G) changes, the DIBL value will also change. The longer the channel length, the smaller the DIBL value. Comparing the DIBL values of the SOI FinFET shown in Figure 6 (a) and BULK FinFET shown in Figure 6 (b), it can be observed that the DIBL value of the BULK FinFET is greater than that of the SOI FinFET for the same channel length.

Figure 6. The DIBL of SOI FinFET(a) is better than Bulk FinFET(b).

4. Conclusion

In this study, the results are simulated by using the ISE TCAD software, and changing a variety of parameters to simulate in different situations. Then, we use the simulation diagram to compare the characterization between SOI FinFET and BULK FinFET. As a results, through the result of the simulation, we can observe that the characteristics of SOI FinFET are better than BULK FinFET.

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5. References

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