120V Low Side LDMOS Device with Sided Isolation of 0.35 μ m CMOS Compatible Process

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Abstract. In this paper, a novel 120V multiple RESURF lateral double-diffused MOS (LDMOS) transistor with shallow trench isolation (STI) structure in low side is developed and successfully simulated. The proposed multiple RESURF LDMOS is able to achieve better ESOA performance while maintaining a benchmark specific on-resistance with breakdown voltage over 120 Volts. The key feature of this novel device is linear p-top rings which are located in the n-drift region. Optimization of p-top mask design and n-drift region concentration is performed in order to achieve the lowest on-resistance possible with the desired breakdown voltage.

1 Introduction

LDMOS transistors are widely used in smart power technologies; Applications are mainly in display drivers, power switching, digital audio and power management devices etc. Now a day, the n-channel lateral DMOS transistor (NLDMOS) is one of the best choices for high voltage device. The focus is to optimize and improve the LDMOS device design to obtain power switches with very low specific on-state resistance (R_{sp}) while maintaining the high switching speed.

LDMOS can be easily integrated into a CMOS or a BiCMOS process which facilitates the fabrication of control, logic and power switches on a single chip [1,2]. Also, for this voltage range, an optimized LDMOS is much more efficient in terms of on-state voltage and switching losses compared to a power bipolar junction transistor (BJT) or other hybrid MOS bipolar devices [3]. Advantage of NLDMOS is that it can be easily integrated without significant process changes and within existing technologies [4]. In order to broaden the applicability of NLDMOS, it is necessary to enhance the electrical performances, such as breakdown voltage, low on-state resistance, and high current driving capability [5]. Since many years, experiments were carried out to improve Breakdown voltage and on-state resistance [6][7].

This paper discusses (how far NLDMOS can be used) with the limitation of the NLDMOS in terms of breakdown voltage and on-state resistance. In this paper, the NLDMOS structure is with the concept of multiple RESURF and linear P-top ring. Based on the simulation experiments 120V Low Side is obtained with

Benchmark on-state resistance of 119.5 m Ω mm² (R_{sp}). Double and multiple RESURF methods [8] had been developed instead of single RESURF technology to improve the junction weak avalanche leakage at high electric field regions and additional layer of opposite conductivity (p-top layer) is incorporated inside the n-drift region. The main purpose of this structure is to increase the optimum charge in the drift region without reducing breakdown voltage for obtaining high breakdown voltage and low specific on-state resistance requirements in conventional NLDMOS devices. The P-top mask was optimized to get the highest breakdown with Lowest on-state resistance (R_{sp}) possible by increasing current-driving capability in the drift region [9–10]. Figure 1 shows the schematic view of new N-channel LDMOS structure with side isolations in front view and in top view.

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Fig. 1. Schematic view of new N-channel LDMOS Structure with side isolations (a) Front view and (b) Top view

2 Materials and methods

The device structure is designed with side isolation techniques to reduce the NPN beta, thereby to avoid the Kirk effect and reduce the leakage current.

Fig. 2. Boron profile of proposed NLDMOS (a) Boron profile Front View (b) Cut line profile for Linear P-top

Figure 2(a) shows the Boron profile of proposed NLDMOS with STI regions and both sides of the N-drift region which is performed by Sentaurus process simulation. For lowering our NLDMOS on-resistance it is very important to improve doping in the n-drift region. Our proposed structure has optimized concentration in n-drift region and an additional layer of opposite conductivity (p-top layer) is included in the n-drift region. The RESURF LDMOS device with linear p-top is shown in figure 2. Linearity of p-top can be seen from the Figure 2(b). The main purpose of P-top in the n-drift

region is to maintain the best charge balance in the drift region of the structure without reducing breakdown voltage. The Linearly Varying Doped (LVD) p-top layer with optimized mask and doping for a RESURF LDMOS has been utilized and proposed, which can improve the influence of inter-connection related breakdown better than conventional RESURF structure. It is clear from the figure that the P-top layer is placed in the n-drift region in order to create more p-n charge. For process conditions, the p-type $\langle 100 \rangle$, background doping of about $6 \times 10^{14} \text{ cm}^{-3}$ was used in an oriented silicon substrate. An epitaxial process of 0.6 μm thickness film in N-type layer was developed on Si substrate with a doping concentration around $5.17 \times 10^{16} \text{ cm}^{-3}$.

3 Results and discussion

Simulations were carried out to obtain the desired breakdown voltage of more than 120V for Low side NLDMOS device structure, which have the lowest on-state resistance possible. In order to obtain the desired breakdown voltage and the lowest specific on-resistance, the n-drift region and p-top rings mask and charges has been optimized in several conditions. Figure 3 shows the breakdown curves for the proposed NLDMOS devices. The on-state resistance of proposed structure is better than 0.13 μm , 0.18 μm , 0.25 μm technologies which were proposed before.

Fig. 3. Breakdown Curve for proposed Low Side NLDMOS device

Fig. 4. Impact-ionization field of Low Side NLDMOS device

Figure 4 shows 3D simulation the surface impact-ionization field distributions along the drift region of the device. The structure has better SOA performance and there is no Kirk effect and saturation point. Figure 5 shows the SOA performance of our device, for gate voltage which justifies our result.

Fig. 5. I-V curves for our proposed NLD MOS structure for different gate voltage

Proposed NLD MOS structure is simple and cost-effective CMOS compatible process with side isolation, have 120V breakdown and better benchmark on-state resistance. By utilizing linear P-top in the n-drift region, we can able to achieve better charge balance in the drift region of the structure which help to reduce the on-state resistance.

Fig. 6. Comparison of Benchmark curves of different technology

4 Conclusion

This device structure is very competitive to achieve the desired benchmark breakdown and on-resistance. This device structure has better impact-ionization, so hot carrier reliability life can be longer. So, we believe that this device structure can be used for future auto-electronics industries and applications.

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