Design of a Low on Resistance High Voltage (120V) Novel 3D NLDMOS with Side Isolation Based on 0.35um BCD Process Technology

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Abstract. High performance power device is necessary for BCD power device. In this paper, we used 3D Synopsis TCAD simulation tool Sentaurus to develop 120V device and successfully simulated. We implemented in a conventional 0.35um BCD MOS process to present of a novel high side 120V LDMOS have reduced surface field (RESURF) and Liner p-top structure with side isolation technology. The device has been research to achieve a benchmark specific on-resistance of 189 m Ω -mm² while maintaining horizontal breakdown voltage and vertical isolation voltage both to target breakdown voltage of 120V. In ESOA, we also proposed a better performance of both device without kirk effect.

1 Introduction

Recently, BCD MOS (Bipolar-CMOS-LDMOS) process is extensively used in variety of areas such like LED Driver, Switching Regulator, Battery IC, Audio Amplifier, Motor Drivers, large displays (TV and monitor), Power Management products, and storage controller chips [1]. One of the most common power switches used for Power IC technologies is the Lateral Double Diffused Metal Oxide Semiconductor (LDMOS) power transistor. The LDMOS provides the advantage of process compatible to VLSI process and is easy to integrate with logic IC or other devices. For power device, a lot of research on the specific on-resistance improvement of LDMOS device have been reported, because specific on-resistance is critical to device performance. Reduced Surface Field LDMOS (RESURF) has been proposed a better to optimize specific on-resistance. Double and multiple RESURF methods [2, 3] had been developed instead of single RESURF technology to highly utilize to improve the specific on-resistance and the junction/weak avalanche leakage at high electric field regions and reduce hot carrier injection into the dielectric in the aims of obtaining high breakdown voltage.

Since the source of a high-side LDMOS tied to the load, the source potential can be higher than the substrate potential while for a conventional LDMOS structure, the source electrode is always tied to the substrate. To implement high-side LDMOS in a conventional BCD process, the NBL (n+ buried layer) has to be located

beneath the LDMOS source region to prevent punch-through breakdown between the source and the p-substrate [4]. The voltage capability of high-side LDMOS depended on junction isolation voltage of NBL junction. This design challenge was not only obtained the horizontal breakdown voltage, but also vertical isolation voltage maintained target breakdown voltage simultaneously.

2 Methods and simulations

Figure 1(a) shows the schematic of a novel 3-dimensional and a single P-top layer NLDMOS structure with STI regions on both sides of the N-drift region which is performed by Sentaurus process simulation. In the cross-sectional view of the proposed high-side 120V n-LDMOS. The NBL should be used to prevent the

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vertical punch-through breakdown between the source and the p-substrate. Because of the use of NBL, the breakdown voltage of the high-side LDMOS can endure higher than that of the low-side LDMOS when source tied to load. The main reason was built an isolation layer that provided punch-through breakdown more than 120V between the source and the p-substrate. Figure 2 (b) to (c) show the front and top views, respectively.

Fig. 1. Schematic of (a) 3D single P-top layer RESURF LDMOS (b) front view (c) top.

It clearly shows that a liner P-top layer is performed in the top of the N-drift region. The liner P-top layer is placed at the top centre of the N-drift in order to create more p-n junctions which will help increase the breakdown. LDMOS was integrated into the standard BCD process. Normal p-type silicon substrate with resistivity of 10-20 Ω -cm was used. For process conditions, the p-type background doping of about 1.3×10^{14} cm⁻³ was used in an oriented silicon substrate. An epitaxial process of 0.6- μ m-thickness N-type layer was performed on Si substrate with a doping concentration around 4.65×10^{16} cm⁻³. In addition, a variety of the width area ratio of WN-drift/WSTI were a crucial factor which applied to obtain the optimal performance.

Fig. 2. LBV, Ron vs WN-drift/WSTI Curve.

Fig. 2 shows the off-state breakdown voltage and specific on-resistance curves as a function of different

ratio of WN-drift/WSTI respectively. It is clearly seen the 6.14 ratio of WN-drift/WSTI has much better on-resistance and breakdown voltage compared to other ratios. The WN-drift/WSTI ratio significantly influences the device breakdown voltage and specific on-resistance. Because a large WN drift/WSTI ratio can obtain more breakdown voltage, but the specific on-resistance simultaneously degeneration velocity maybe faster than breakdown voltage. It led the device of poor performance.

Fig. 3. The P-top linear profile (a) Boron doping profile (b) Net doping profile.

The mask design of linear P-top layer plays the crucial role in order to achieve target breakdown voltage and the lowest possible specific on-resistance. The P-top layer length, depth and doping concentration of the P-top layer are the key parameters in the Double RESURF LDMOS. The simulation result can be seen clearly in Fig. 3 which is demonstrating linear profile for boron impurity degraded gradually from source side to drain side. The appropriate linear variation of p-top layer can optimize both breakdown voltage and specific on-resistance values. The main purpose of this introduced P-top layer structure is to minimize the on-resistance while attain the desired breakdown voltage, meanwhile the conventional double RESURF and single RESURF structures are not able to achieve that technology value.

3 Results and discussion

Fig. 4. LBV, Ron vs Linear P-top dose Curve

We fabricated the 120V high-side LDMOS transistors in our 0.35 μm BCD process. Simulations executed to obtain the desired breakdown voltage of 120V having lowest Ron possible without using any extra mask. One additional mask layer was used for the surface P-layer. Fig. 4 shows the characteristics of the breakdown voltage and the specific on-resistance are proportional from the linear P-top layer dosage variation. The proposed high-side LDMOS provides a breakdown voltage.

Fig. 5. Experimental IDS-VDS characteristics for 120V high side device

An ESOA of LDMOS device is very critical for power device performance. Fig. 5 shows the forward I_{DS} - V_{DS} characteristics and off-state breakdown voltage for the 120V high-side LDMOS transistors and the device shows a good ESOA performance when $V_G=5V$ achieve high on-state breakdown voltages of $V_{DS}=117V$. Generally, the on-state breakdown voltage of the LDMOS is lower than the off-state breakdown voltage due to Kirk Effect [5]. However, the cause of the Kirk Effect problem mainly due to the high beta value of parasitic NPN transistor in the p-body. Therefore, we must have optimized beta of parasitic NPN transistor for reducing the kirk effect [6]. We can speculate the beta value of parasitic NPN transistor close to equal to 1 when off-state breakdown voltage near on-state breakdown voltages. It will obtain a good ESOA region and without kirk effect for On-state I-V curves.

4 Conclusion

Fig. 6. Trade-off characteristics between the breakdown voltage and the specific on-resistance.

In this paper, 120V high-side LDMOS was implemented in a conventional 0.35 μm BCD process. The proposed LDMOS structure is very competitive to achieve breakdown and benchmark specific on-resistance. The proposed high-side LDMOS provides lateral BV 125V, vertical isolation voltage 135V and $R_{ONsp} = 1.89 \text{ m}\Omega\cdot\text{mm}^2$ with a wide region of ESOA. Based on Fig.6 [7] and these electrical performances, we believe that this novel device has sufficient potential in comparable with previous advanced LDMOS device.

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