An Innovated 80V-100V High-Side Side-Isolated N-LDMOS Device

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Abstract. We used TCAD Synopsys 3D tools and device simulators to propose an innovative device structure of 80V-100V high-side NLD MOS by using the silicon to silicon-di-oxide ratio with side trench. The high-side can also be developed by placing an NBL structure which can deliver a high as over 200V isolation voltage. The 3D structure can clear see the optimized linear p-top and n-drift region have better charge balance with linear doping profile to get the benchmark breakdown voltage (BV_{dss}) of 80V with on-resistance (Ron) as low as 130 mΩ·mm² and 100V with on-resistance as low as 175 mΩ·mm². The linear p-type buried layer using high dosage and lower energy to achieve the better SOA and higher isolation voltage. Optimized linear p-top and PBL can improve Ron by 32.5% compare to other 100V high side device which have done from reference.

1 Introduction

For 50V-140V smart power device is highly demanded by auto and motor driver's industry. In order to get high performance for ESOA and TSOA [1], some study use expensive technology for process and complication of structure that increase cost, such as silicon-on-insulator (SOI), double epitaxial layer [2], use n-well and p-well together etc. Kirk effect show NPN of β issue that is serious for on-state I-V curve and affect ESOA performance [3].

Comparison to low-side, high-side need a best junction isolation breakdown and also sustain the lateral breakdown which use NBL (n+ buried layer) between the source and the substrate. In this work, we propose a new innovated [4] high-side side-isolated n-channel LDMOS 3D device on both front and back edges of the extended drift region with thickness epitaxial layer. A double-RESURF concept incorporates an additional layer (linear p-top layer) [5] inside the n-drift extended region to get the charge balance, the net doping will clear see the linear profile curve, it can improve on-state resistance and keep high breakdown, the good charge balance not only get lower Ron and high breakdown also reduce the device length to cost down.

To avoid the transistor beta, cause the Kirk effect, we use linear p-type buried layer (PBL) [6] on top of n-type layer (NBL) inside the epitaxy layer, the balance between PBL and NBL need to consider the isolation BV can't be destroy, so the linear PBL give the small transistor beta and also make the good profile curve to sustain the high isolation breakdown. The device is 3D

simulation. Each region is optimized by several experiments. The process was optimized using a simulation written in TCAD Synopsys 3D tools to determine.

2 Device structure and conditions

This NLD MOS High Side device in this study is using 0.35μm process with shallow N-epitaxial drift region, simulated with TCAD Synopsys tools and device simulators.

Figure 1 shows our novel device cross section structure, and simulated top view in Synopsys with device length 7.6μm. Table 1 show this work simple condition. For this novel device, channel length of 0.35μm is formed by p-body diffusion doped at $3 \times 10^{17} \text{cm}^{-3}$, drift region is doped at $4.65 \times 10^{16} \text{cm}^{-3}$, and source and drain contacts are all doped at $1 \times 10^{19} \text{cm}^{-3}$.

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The gate oxide composed of SiO_2 is 120Å thick with a gate length of $0.75\mu\text{m}$.

Fig. 1. Schematic of 3D (a) High-Side Side-Isolated N-LDMOS proposed structure; (b) top view; (c) front view; (d) rotation view.

Table 2. The parameters which using in the TCAD Synopsys 3D simulation.

Parameters	Unit	Values
Substrate	ohm-cm	100
N-epi	ohm-cm	0.145
Epi thickness	um	0.6
p-body	cm-2	$3e^{13} \sim 3e^{14}$
n-type buried layer	cm-2	$5e^{12}$
n-type blanket	cm-2	$7e^{11} \sim 9e^{11}$
Source contact	cm-3	$1e^{19}$
Drain contact	cm-3	$1e^{19}$

The key technique that implemented in this work are linear highly doped with lower energy of p-type buried layer and linear p-top region. The linear highly doped of

p-type buried layer using high dosage and lower energy to get the charge balance in the deep n-type buried layer, the doping profile showed in figure 2, the linear curve can provide high isolation breakdown also make the better SOA.

Fig. 2. Linear p-type buried layer and n-type buried layer doping profile, the curve present not only in boron profile also net doping profile have good linear trend.

The linear p-top made the good charge balance and present the linear doping profile in the n-drift region showed in figure 3, the linear trend curve redistribution the surface charge to make the high breakdown also improve R_{ON} .

Fig. 3. Linear p-top region has good charge balance in N-drift region, the profile in different location all have linear trend curve.

3 Result and discussions

3.1 Device breakdown and SOA

From double RESURF concept, we put the p-top of shallow region in the n-drift region surface in our novel device. P-top region have a linear trend curve relationship with the n-drift region for charge balance. This linear trend curve not only get the high lateral breakdown but also have benchmark on-resistance.

For the High Side structure, we placed the N-buried layer under the source side. The shallow n-drift region cannot make a good sensitivity for P-buried layer and N-

buried layer. In order to maintain a good isolation breakdown and reduce the beta of the parasitic NPN transistor, we innovate the linear p-buried layer. There by, the device has low leakage current and avoid on-state curves of Kirk effect. It not only can improvement the SOA curve but also have the good isolation breakdown as we can see in Figure 4.

Fig. 5. I_d vs. V_d characteristics of device for (a) 80V and (b) 100V High-Side Side-Isolated NLD MOS of off-state breakdown voltage at $V_g=0$ and on-state breakdown voltage at $V_g=4V$ and $V_g=5V$ in 3D simulation

3.2 Optimized characteristics of device

In order to consider the cost and charge balance, this paper of 80V-100V High-Side Side-Isolated NLD MOS device use the same size of device length, width and height. To analysis simulation of result, figure 6 shows that adjustment phosphorus dosage of n-blanket for our innovated 80V-100V High-Side Side-Isolated NLD MOS device design.

The curve of relationship can observe more phosphorus dosage of n-blanket that lateral breakdown voltage and R_{on} decreasing in direct proportion; otherwise increasing. In this work, for our 80V High-Side Side-Isolated NLD MOS use $9e11$ of n-blanket dosage can get 81.8V of lateral breakdown voltage and R_{on} is $112 \text{ m}\Omega \cdot \text{mm}^2$. For 100V voltage use $7e11$ can

get 101V of lateral breakdown voltage and R_{on} is $118 \text{ m}\Omega \cdot \text{mm}^2$.

Figure 7 shows the result of breakdown voltage and on-resistance compare with some of the conventional high-side NLD MOS and this work has the best R_{on} for 80V-100V.

Fig. 6. Both of the off-state breakdown voltage and on-resistance curves as a different N-blanket dosage for innovation 80V-100V High-Side Side-Isolation NLD MOS device.

Fig. 7. Trade-off characteristics between the breakdown voltage and the specific on-resistance.

4 Conclusion

The 80V-100V High-Side NLD MOS with Sided-Isolated structure still produce high R_{on} due to the drift length limit. The newly invented device structure using short drift length with sided isolation can deliver high lateral breakdown and high isolation breakdown as well with low R_{on} . We implemented NBL (n+ buried layer) which to be located beneath the source region to prevent punch-through breakdown between the source and the p-substrate, also get high isolation breakdown without affecting other characteristics. In addition, the device with added linear p-type layer and linear p-top can reduce Kirk effect and get high breakdown with better low R_{on} .

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