Study of HCI Reliability for PLDMOS

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Abstract. In this paper, we demonstrate electrical degradation due to hot carrier injection (HCI) stress for PLDMOS device. The lower gate current and the I_{Dsat} degradation at low gate voltage (V_{GS}) and high drain voltage (V_{DS}) is investigated. Hot Electrons, generated by impact ionization during stress, are injected into the gate oxide, creating negative fixed oxide charges and interface-states above the accumulation region and the channel. Increase of the drain-source current is induced by the negative fixed oxide charges. The physical model of the degradation has been proven combining experimental data and TCAD simulations.

1 Introduction

Most of the studies about hot-carrier effects concentrated on n-MOSFETs rather than p-MOSFETs simply because the hot-carrier induced problems are more serious in n-MOSFETs due to longer mean free path, hence higher energy of electrons. For example, peak substrate current in n-MOSFETs is about 3 to 4 orders larger than in P-MOSFETs. In near-micrometre CMOS integrated circuits, N-MOSFETs are known to fail earlier than P-MOSFETs. However, the empirical relationship between P-MOSFET DC lifetime and lifetime monitor is usually obtained over narrow V_{GS} ranges, for example V_{GS} near the peak of I_{Sub} or I_{G} , and may not be suitable for lifetime modeling for arbitrary stressing waveforms. A general expression which can well describe device degradation over a wide range of bias is thus required. In the following, hot-carrier-induced degradation and gate current model in SC p-MOSFETs are presented. The lifetime of a SC p-MOSFET is found to correlate with I_{G} over a wide range of V_{GS} . Using this correlation and a gate current model based on the lucky electron approach, the lifetime of a SC p-MOSFET under pulse stress can be estimated [4].

However, the use of power semiconductor devices is exponentially growing, because increased efficiency is required in energy conversion process and better circuit solution is continuously proposed. One of the strongest motivations for research in this field is the largest market segment of automotive body control power. In some cases, P-channel power devices can be a better option than the n-channel devices, when the lower performance of the PLDMOS (i.e. Lower switching speed and higher RON) can be less important than the possibility of

significant circuit simplification. The new rising market of LED driver for automotive interior and exterior lights, LED daytime running lights and LED front lights is a typical example. One of the key devices in this product is the PLDMOS, which is, for example used in the low-dropout (LDO) regulator of the converter. A low-dropout or LDO regulator is a DC linear voltage regulator, which can operate with a very small input-output differential voltage. The substitution of the bipolar device with the PLDMOS transistor leads to several advantages such as a lower minimum operating voltage, higher efficiency operation and lower heat dissipation. In this case, the use of the n-channel lateral DMOS transistor would need some more circuitry and cannot be used in open loop conditions [2].

2 Experimental setup

The experimental setup was designed as flowchart in Fig.1 (b). Practically, the comparisons of the device degradation are performed by confrontation of the IV curve before and after stress time on the device structures. Thus, degradation trend for drain current saturation (I_{Dsat}) were calculated for different stress time until we will get 2% of I_{Dsat} degradation. Before that we have measured V_{gmax} from I_{G} - V_{G} curve at -40V of drain voltage and -5V of gate voltage. According to that we were selected V_{gmax} and the stress voltage -40V of V_{DD} . After stress, the drain current saturation calculated at 40V of drain and selected gate voltage (V_{gmax} from I_{G} - V_{G} curve).

Degradation, thermodynamic HCI and classical lucky electron models were invoked in the device simulation to

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perform the interface trap generation due to HCI. A process of electrons tunnel through a barrier in the presence of a high electric field was taken into account by using Fowler-Nordheim model. While, the lucky-electron model provides an estimate of the probability that some carriers in silicon will be transmitted to the oxide by overcoming the local energy barrier at the Si-SiO₂ interface [5-7].

Fig. 1. (a) Simulated structure of new proposed PLDMOS structure (b) Flowchart of the experimental design.

3 Gate current model

Since, gate current is a better monitor than substrate current for device degradation in p-MOSFET's modelling of gate current is important. Unlike n-MOSFET's, p-MOSFET's exhibit the largest gate current when biased in the saturation region at low V. The gate current has a long mean free path. Also, the Si-SiO₂ barrier height is lower for electrons and the vertical field at low VG favours electron injection [4].

4 Results and discussion

Simulations As we are shown in Fig 2, we have measured VGmax from different devices and we have plotted Ig-Vg curves from different devices. The VGmax was measured at V_{DD}=-40V and V_g=-5V. We have found lower Igmax for device4 as shown in Fig 2. This Igmax was better than other devices. From this Igmax curve, we have measured VGmax. So, as we know HCI degradations is because of trapped charges into the oxide

region of Si/SiO₂ interface and HCI degradation will be more with more traps that occurs in oxide regions. We perform HCI stress test for them until that device reaches 2% of ID_{sat} the degradation and measured drain saturation current shift (Δ ID_{sat}) at V_{DD}=-40V and selected gate voltage from gate current curve and we summarize all HCI results with different condition device performances. When we analyse the results, we can explain that the lower gate current device has very good HCI performance. We have proved our device lifetime, improved according to the gate current measurements. The comparison life time curves between device Life Time(Years) Curve Between Stress Time (Sec) and ID/ID (%) shown in Fig 3. It is possible for us to achieve this HCI performance because we put lots of effort to redesign the device so that impact-ionization hotspot should happen at a location away from the gate and below the surface so that the hot carriers that generate and experience high lateral applied field should not reach or overcome the Si/SiO₂ potential barrier and become trapped into gate-oxide region. So we kept this in mind and re-designed our device which helps to get better HCI performance and device can pass HCI life time reliability test.

The increasing rate of Δ ID/ID with stress-time becomes small after extended stress. Extrapolating the short-term stress data to obtain device lifetimes can introduce large errors. To avoid this, we stress the devices long enough so that, Δ ID/ID exceeds or nearly reaches the lifetime criteria. τ is defined as the time at which Δ ID/ID reaches a certain percentage (2-4%). The devices were stressed with fixed V_D, and varying V_G. In both cases, the correlation can be expressed as $\tau \propto I_G^{-m}$ with $m = 2.25$ as shown in Fig 4.

Fig. 2. Comparing Curves between Gate Voltage v/s Gate Current.

Fig. 3. Device Life Time(Years) Curves Between Stress Time(Sec) and ID/ID (%).

Fig. 4. Device Life Time(Years) Curves Between Stress Time(Sec) and I_{gmax}

Table 2. Different Stress Time (Sec) and IDs at degradation shift (%)

	Device-1	Device-2	Device-3	Device-4
Stress Time (Sec)	$\Delta ID/ID$ (%)	$\Delta ID/ID$ (%)	$\Delta ID/ID$ (%)	$\Delta ID/ID$ (%)
1.00E+05	0.23	0.25	0.2	0.16
1.00E+06	0.83	0.90	0.76	0.614
6.93E+06	1.77	1.94	1.63	1.41
9.46E+06	1.93	2.12	1.80	1.60
1.10E+07	2		1.90	1.75
1.30E+07			2	1.87
1.40E+07				1.95
1.45E+07				2

It's clear from the table that the device with the lowest I_g current have the maximum life time. And as the I_g current increases the lifetime of the device degrades.

5 Conclusion

Some of the hot carriers generated in the bird's beak area are injected into the gate oxide and the others constitute the substrate current. The majority of hot carriers injected into the gate oxide is collected by the gate electrode and constitute the gate current. Both of the gate current and substrate current are a good monitor to predict device degradation. While gate current is a direct measurement of the injected carriers into the gate oxide, it is very sensitive to the trapping mechanism (during TCAD simulation) and is very low. In our present work, we measured gate current and it makes easier to measure. Although high-voltage LDMOSFETs have a large depletion area in the drift region (large part of the generation current by impact ionization in this region constitutes a gate current), gate current is an indirect way of measuring the hot carrier injection.

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