Sensitivity Study of Polysilicon Nanowire Based on Scattering and Quantum Mechanics Models

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Abstract. In this paper, we report nanowire drain saturation current sensitivity property to measure femtomol level change in drain current due to different proteins i.e. DNA with numerical simulation and fabricated polysilicon nanowire based on the theoretical predictions. In addition, the drain current will also be affected by the back-gate voltage and will increase as the back-gate voltage increases. A 3-dimensional Synopsis tool is used to investigate the drain current behavior for a polysilicon nanowire. The scattering compact model reported result of detailed numerical calculation shows in good agreement, indicating the usefulness of scattering compact model. Whereas 3D synopsis unable to explain the whole region of the drain current characteristics in linear region which uses quantum mechanics model approach.

1 Introduction

Nanowire (NW) have attracted wide attention, and analyses that focus on various aspects of the device operation have accumulated. We have offered an experimental and analytical method to observe the polysilicon NW MOSFET threshold voltage based on a simple ballistic MOSFET modeling from the private communication with Natori. [1] In previous paper we proposed scattering effects into the ballistic modeling and to provide a compact model of the quasi-ballistic Si NW MOSFET. Now our current study compares the two different approaches of physics to study the electrical characteristic of device. Based upon Sentaurus device simulation which uses quantum mechanics approach and theoretical study of semi-classical physics. Silicon NW MOSFETs attract wide attention as a promising Nano device for future high-density LSI application. For development of the device including the circuit application, a handy tool that affords accurate prediction of device characteristics is indispensable.

Semiconducting silicon nanowire field effect transistors (SiNW FETs) have been shown to function as transducers for label-free, high-sensitivity and direct electrical detection of biomolecules.[1][4] The ultrahigh sensitive detection can be attributed to their small size and large surface-to-volume ratio, enabling local charge transfers to result in a current change due to a field effect, such as when the analytical molecules bind to specific recognition molecules at the surface of the nanowire. This effect is sufficiently strong that single charge at the

surface of the nanowire can be sensed because the depletion or accumulation of charge carriers affects the entire cross-sectional conduction pathway of these nanostructures. [5]

2 Device fabrication approach

2.1 Bottom up Fabrication approach

A simple and low-cost method to fabricate polycrystalline silicon (poly-Si) NW FET for bio sensing application has been demonstrated [6][7]. The poly-SiNW channel can be fabricated by employing the poly-Si 'bottom up' process, in an approach which is compatible with current commercial semiconductor processes. Throughout the fabrication, no expensive lithography tools are needed for definition of the nano-scale patterns. The fabricated devices exhibited good performance and showed great potential to be developed to an ultrasensitive biosensor because of their excellent electrical characteristics in aqueous solution. [8]

2.2 Fabrication steps

The device samples were manufactured on standard 6-in. p-type wafers. A proposed hybrid sensor/memory/CMOS poly-Si nanowire structure is illustrated in Figure 1. The bottom-gate poly-Si

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nanowire formation can be inserted specifically after metallization of the back-end process (BEOL).

Fig. 1. Optical microscope image of nanowire device.

At the beginning, buried oxide was deposited on a substrate surface as the gate dielectric of nanowire FETs. A 50-nm polysilicon layer was then deposited using the CVD process. Subsequently, the poly-Si wire was patterned by the standard I-line stepper of the CMOS semiconducting process. By using reactive plasma etching for photoresist trimming followed by silicon etching, the NW dimension was scaled to a level of approximately 100 nm. Figure 2. Showed the zoomed view of Nanowire.

Fig. 2. Zoom optical microscope image of nanowire device.

A NW shrinkage technique using poly re-oxidation and oxide stripping was employed to scale down the NW width to less than 50 nm. A channel protection photoresist pattern was then formed by I-line lithography.

Fig. 3. 3D Cross-section of the simulated device.

Figure 3. Show the 3D cross section of the simulated device. The objective of the channel protection patterning was to keep the channel intrinsically from n+

source/drain (S/D) implantation, to increase NW FETs sensitivity. Subsequently, the n+ S/D implant was performed with a $5 \times 10^{14} \text{ cm}^{-2}$ arsenic ion beam at 10 KeV to reduce the parasitic resistance of the NW. Thereafter, the channel protection photoresist was removed. Finally, the S/D dopant was activated by annealing treatment at 600 °C for 30 min in a N_2 ambience.

3 Simulation methodology

Simulation is one of the stages that are important before manufacturing device. In simulation, the device can be analysis the optimal functionality and the performance. By using simulation tool, it allows the user produce the prototype even the device become more complex and become more difficult to do experimentally. Simulation program will reduce the time and enable the researcher from the based on the concept of the chip potential and their characteristic performance.

In this paper, the result of polysilicon nanowire is observed for the conductance of the device. The simulations of the model design characterized are using the boundary conditions as described in our previous study. In our simulation, various simulation models have been used to match the silicon result.

In this study, a simulation methodology is presented based on a 3D drift diffusion (DD) simulator including quantum confinement effects to accurately describe the electrostatics related characteristic. But the simulation tool fails to explain the Id-Vg curve in all regions i.e. also the simulation results fits only in the saturation region, but fails to explain the linear region of the curves.

The drain current is readily evaluated by following a simple procedure if device parameters and bias conditions are specified. A comparison with a reported result of detailed numerical simulation [4] showed good agreement, indicating the usefulness of the compact model. The compact model includes the energy integration as well as the sub-band summation, and numerical procedures are inevitable for the detailed evaluation. But here, we introduce some reasonable approximations in the NW structure and the carrier statistics in the compact model, and intend to derive analytic expressions of the device current.

Fig. 4. Comparison of the three Id-Vg curves for simulation result, compact model curve with the fabricated silicon chip at drain biased at 3V.

Also, our compact analytical equation for the drain saturation current derive the injection velocity equation for the fully degenerate condition. And can we have calculated with the handy calculation. This drain current formula is obtained from Kenji Natori with the private communication of Prof. Gene Sheu, equation 1. [5]

$$I_D = C_G(V_G - V_t)V_{inj} \frac{(1-R)\left\{1 - \exp\left(-\frac{qV_D}{k_B T}\right)\right\}}{(1+R) + (1-R)\exp\left(-\frac{qV_D}{k_B T}\right)} \quad (1)$$

$$V_{inj} = \frac{I_d}{C_{eff}(V_G - V_t)} \times \frac{(1+r) + (1-r)\exp\left(-\frac{qV_d}{k_B T}\right)}{(1-r)\left\{1 - \exp\left(-\frac{qV_d}{k_B T}\right)\right\}} \quad (2)$$

The above equation we propose for the injection velocity calculation for the fully degenerate condition, in non-degeneracy condition the injection velocity supposed to be constant as shown in equation 3. [9]

$$v_{inj} = \sqrt{\frac{2k_B T}{\pi m_x}} \quad (3)$$

Also, we take the Vinj curve as a reference from the Purdue University, they have quantum mechanics approach to solve for the Vinj equation but also our equation derived from the compact model [9] as shown in equation 1 can also be able to calculate the injection velocity.

Fig. 5. Red line is the reference line from Purdue University and blue line is our work proposed equation for Vinj for higher drain biased voltage at 5V

4 Conclusion

Nanowire drain saturation current sensitivity property to measure femtomol level change in drain current due to different proteins i.e. DNA with numerical simulation and fabricated polysilicon nanowire based on the theoretical predictions. In addition, the drain current will also be affected by the back-gate voltage and will increase as the back-gate voltage increases. A 3-

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