Deep sub-micron ESD GGNMOS layout design and optimization

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Abstract. In the field of integrated circuits, ESD (Electro Static Discharge) has always been a rather serious problem of reliability. Enhanced ESD tolerance of IC chips became a focus of research on IC failure protection design. The thesis is better to solve the multi-fingered non-uniform conduction of ESD devices under electrostatic pulse. Layout parameters DCGS (Drain-Contact to Gate Spacing), SCGS (Source-Contact to Gate Spacing) and BS (Substrate-source spacing) size in the paper can be used as reference for ESD GGNMOS (Gated Ground NMOS) layout design. Also this paper provides setting the DRC (Design Rule Check) command to check the distance between the N+ diffusion regions of different potentials so that ESD failure is prevented effectively. TLP (Transmission Line Pulse) current pulse signal is adopted to measure characteristics of the GGNMOS. The thesis descripts a ESD Optimal layout design from five aspects of introduction, Key elements of ESD circuits layout design, ESD layout optimization, a ESD GGNMOS layout instance and conclusion.

1 Introduction

There are two kinds of failures caused by ESD: One is the thermal failure caused by excessive current; the other is due to the high voltage which causes the electric effect to cause breakdown of the medium (such as gate oxide). The thermal failure is, because the local current excessive concentration, causing a large number of heat accumulation, resulting in metal interconnection or semiconductor melt, further lead to two breakdown, the damage mainly concentrated in vias, diffusion resistance, poly-silicon resistors and metal wires. The electrical failure is the ESD voltage applied directly to the vulnerable thin oxide layer, leading to dielectric breakdown or surface breakdown. A variety of reasons have led to the failure of the chip under ESD pulse. These reasons may be due to the inappropriate layout design [1], parasitic ESD devices, the internal ESD sensitive circuit structure and the incorrect placement of the power pins.

2 Key elements of ESD circuit layout design

In deep submicron CMOS (Complementary Metal-Oxide Semiconductor) technology, ESD protection circuits protect Integrated circuit from high current or high voltage attacks, usually are very larger, in order to achieve the I/O input and output ESD protection, power clamp protection, and rail to rail ESD protection. GGNMOS with large $\boldsymbol{W}/\boldsymbol{L}$ ratio is generally designed with multi-finger layout. Under ESD pulse, the biggest problem is the non-uniform conduction of large size multi-finger transistors [2]. Secondly, in the high density unit chip, the parasitic NPN transistor exists, Under ESD pulses, parasitic NPN transistors may be triggered by substrate current, resulting in ESD failure [1]. Therefore, in the layout design of large size GGNMOS, we must solve the key multi-finger transistor layout, as far as possible to ensure the GGNMOS uniform conduction, or through the layout structure design to improve it the breakdown voltage of two $\boldsymbol{V}_{t2}$, avoided premature thermal breakdown; At the same time, by checking DRC validation command in the layout design rule, the space between the N+ diffusion regions of different potentials in the I/O unit is examined to avoid it too small to induce NPN turn-on.

3 ESD layout optimization design

3.1 GGNMOS multi-finger structure and optimization of layout design parameters

The channel length $\boldsymbol{L}$ (Length), channel width $\boldsymbol{W}$ (Width) and even multi-finger number n of the MOS device have been determined in the GGNMOS layout design. Therefore, it is the key to solve the layout design of GGNMOS multi-finger structure, DCGS, SCGS and BS, these GGNMOS structural parameters as shown in Figure 1.

In deep sub-micron conditions, increasing the channel length $\boldsymbol{L}$ does not improve the withstand voltage of GGNMOS leakage voltage [3-5]. Therefore, the channel length $\boldsymbol{L}$ is usually designed to be 0.5μm-0.8μm in length. When designing $\boldsymbol{W}=n\boldsymbol{W}_{UNIT}$ with multi finger, the Fingered-Width $\boldsymbol{W}_{UNIT}$ usually cannot exceed 50μm, and the number of fingers n uses even value [1], [4], [6].

Therefore, the key in design to solve the layout design of GGNMOS multi-fingered structure is DCGS, SCGS and BS, as shown in Figure 1 GGNMOS structural parameters [2, 7].

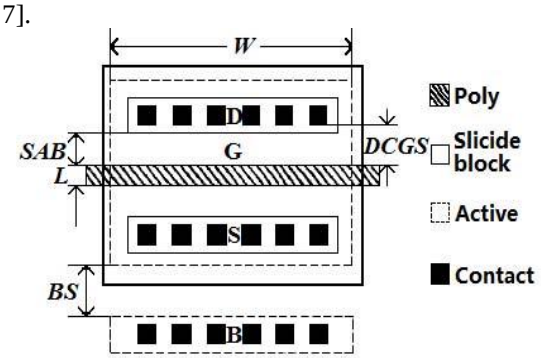
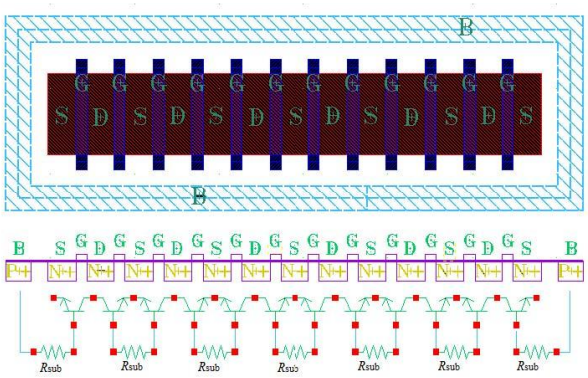
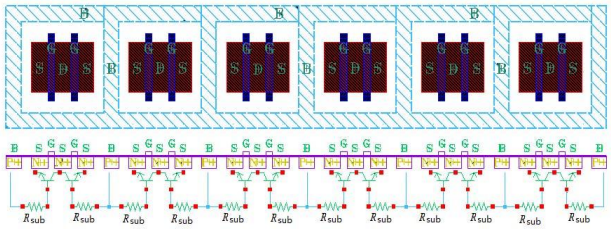


Figure 1. The layout parameters of MOS device.



(a) BSGDGSGDGSGDGSGDGSGDGSGDGSB



(b) BSGDGSBSGDGSBSGDGSBSGDGSBSGDGSBSGDGSB

Figure 2. GGNMOS multi-fingered structure.

The GGNMOS multi-fingered structure is usually designed with S (Source) - S merging and D (Drain) -D merging. And then the source and drain metal lining leads a multi-fingered structure, which is compact, but the problem of non-uniform conduction is serious, as shown in Figure 2(a). In deep submicron process, in order to solve the inhomogeneous conduction problem, instead of using BSGDGSGDGSGDGSGDGSGDGSGDGSB layout as shown in Figure 2(a), GGNMOS is designed with BSGDGSBSGDGSBSGDGSBSGDGSBSGDGSBSGDG SB layout as shown in Figure 2(b), which has better uniform conduction performance. In Figure 2(b), the substrate resistance $\boldsymbol{R}_{sub}$ of each parasitic NPN composed of NMOS Drain, Source and P-sub substrate is the same, which ensures uniform conduction under ESD pulse; Whereas As shown in Figure 2(a), the substrate resistance $\boldsymbol{R}_{sub}$ is larger due to the resistance of the substrate $\boldsymbol{R}_{sub}$ on both sides of the substrate is half of the adjacent substrate resistance. And the intermediate substrate resistance $\boldsymbol{R}_{sub}$ is largest. On the ESD pulse, it cause inhomogeneous conduction that the middle parasitic NPN conducting but side parasitic NPNs not, substrate resistance is bigger, NPN parasitic is more easy to conduct [8, 9].

Because the GGNMOS device turn-on trigger voltage $\boldsymbol{V}_{t1}$ decreases with the increase of DCGS [4], When the DCGS is 5μm, the maximum secondary reverse breakdown current $\boldsymbol{I}_{t2}$ and the smaller GGNMOS turn-on voltage $\boldsymbol{V}_{t1}$ can be obtained. The size of DCGS is a key factor that can affect the performance of GGNMOS.

With the decrease of SCGS, the $\boldsymbol{V}_{t1}$ and $\boldsymbol{I}_{t2}$ show an increasing trend, which is not conducive to the effective triggering of LNPN so that SCGS can consider the minimum design size [4].

As the $\boldsymbol{V}_{t1}$ decreases with the increase of BS, this is beneficial to the effective triggering of the LNPN structure of GGNMOS devices, The $\boldsymbol{I}_{t2}$ shows the lowest peak value at SCGS=4.0μm. Therefore, the design as shown in Figure 2(b) is available in GGNMOS layout.

3.2 Verification of different N+ potential intervals

Because of the N type region of GGNMOS, the N type region with different potential nearby and P-substrate, there will be parasitic NPN transistor. The most simply practical and effective way to avoid parasitic NPN is to increase the spacing of N type diffusion regions with different potentials. By increasing the Base thickness of parasitic NPN transistor, the distance between parasitic NPN emitter junction and collector junction is increased. The minority carrier in Base region cannot be collected in collector region, and parasitic NPN cannot be conducted. Alternatively, the heavily doped P-substrate enhances the threshold voltage of parasitic NPN.

The command can be set in DRC (Design Rule Check) to check the spacing of the N diffusion region with different potentials as follow:

```
ESD.sn.chk.1{
  @enimp of different potential space must >= 4
  EXT enimp< 4 ABUT<90SINGULAR REGION NOT CONNECT
}
```

Among them, enimp is the N type diffusion region with different potentials; NOT CONNECT represents a N type region that is not connected by a metal or other connecting layer; REGION indicates that when the error is found, the range is displayed when the error is displayed; SINGULAR means that a touch or a touch is wrong; ABUT<90 indicates the intersection angle less than 90 degree error. Here, the different potential N type diffusion region minimum spacing is 4μm.

4 A ESD GGNMOS layout optimization model

4.1 ESD GGNMOS optimized layout structure

Layout structure as shown in Figure 3 is part of layout refer of the serials shown in Figure 2(b). The ESD device consists of GGNMOS in which drain D and source S form multi-fingered structure. The gate G is connected with the source S through the metal-contact-poly at the top and

bottom, and the drain D is from the up line. The gate G and the source S are contacted with the substrate, and the B is formed by assembling the lower finger to line below the device.

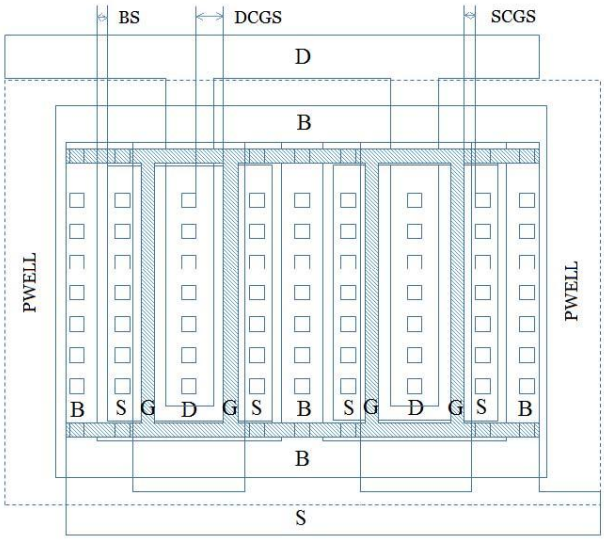


Figure 3. GGNMOS layout structure optimization.

4.2 GGNMOS layout based on 0.13μm process

In this paper, the GGNMOS ESD layout of LDO (Low Drop-Out) regulator chip is completed based on the 0.13μm as shown in Figure 4. And the Figure 4 is the layout of the GGNMOS and bonding-pad. The input and output signals are connected to the PADs, which is formed from the Input PAD into the internal IC circuit and from the internal IC circuit to the Output PADs.

According to the above optimization principle, the GGNMOS layout is optimized that parameters of it are shown in Table 1.

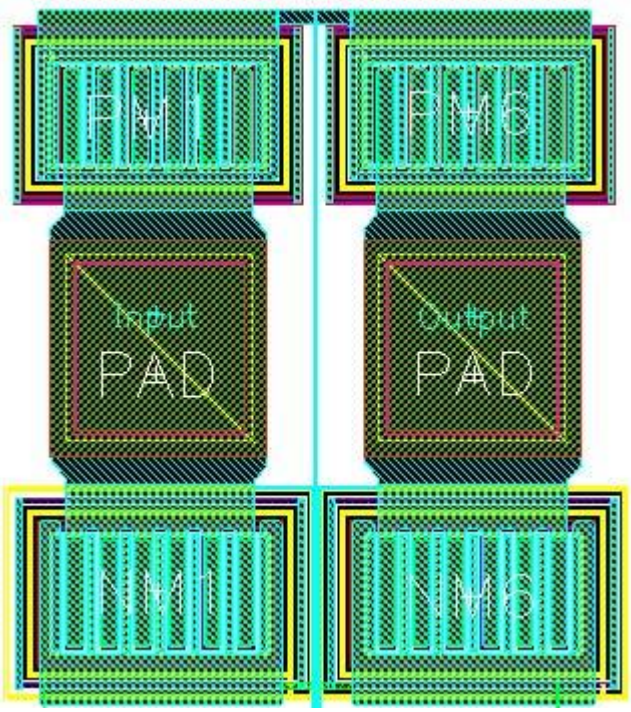


Figure 4. GGNOMS in ESD design.

Table 1. GGNMOS layout design parameters

W_{UNIT}	L_{UNIT}	*Multiple*	DCGS	SCGS	BS
50μm	0.5μm	12	1.8μm	0.63μm	2μm

W_{UNIT} is the channel width of the unit GGNMOS, L_{UNIT} is the channel length of unit GGNMOS, and ***Multiple*** is the number of multi-fingered.

5 Performance after ESD layout optimization

TLP [10-14] current pulse signal, which is 100ns pulse width, 10ns rising time, 10ns falling time and 40mA currents, is added to the drain of the GGNMOS device, at the same time the gate, source and substrate of it are grounded. As shown in Figure 5, the V_D - I_D characteristic is the result of the simulation of the GGNMOS device. It is shown in the Figure 4 that the V_D - I_D characteristic coincides with the snapback obtained by theoretical analysis after GGNMOS layout optimization. It is uniform conduction within the GGNMOS device, because the drain secondary breakdown voltage V_{t2} is greater than the trigger voltage V_{t1} that is about 8*V*. Meanwhile, it is beneficial to GGNMOS triggered conduction, and the drain holding voltage V_h in the diagram is also reasonable. Figure 6(a) is the hole carrier current density, Figure 6(b) is the electron carrier current density. They are shown the internal states near the channel when the GGNMOS is triggered.

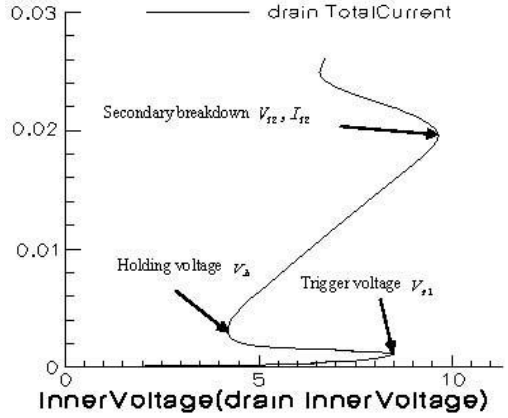
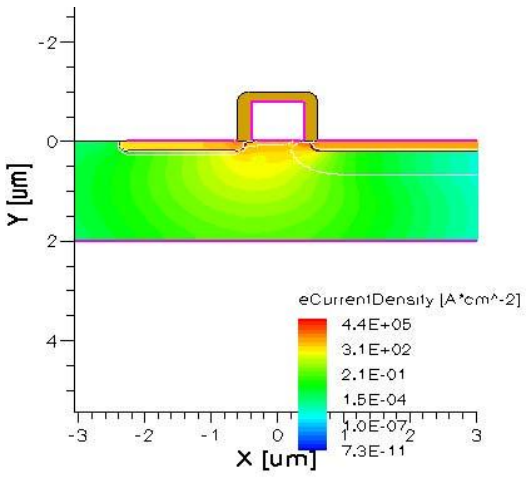
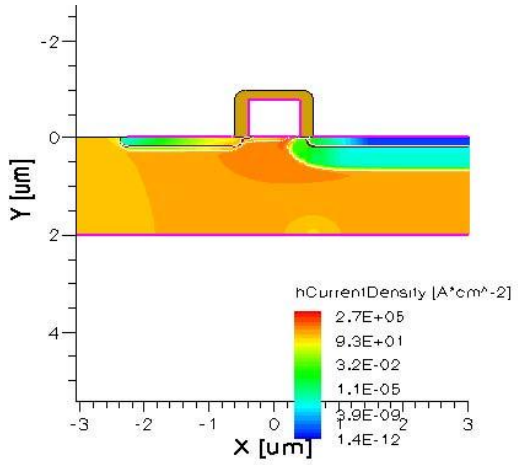


Figure 5. The V_D - I_D characteristic of optimized GGNMOS.



(a) the hole carrier current density



(b) the electron carrier current density

Figure 6. The current density of optimized GGNMOS.

6 Conclusion

In this paper, the GGNMOS layout optimization design of ESD devices is presented. It is better to solve the multi-fingered non-uniform conduction of ESD devices under electrostatic pulse. Layout parameters DCGS, SCGS and BS size in the paper can be used as reference for ESD GGNMOS layout design. The parasitic NPN around the GGNMOS could be found by Setting the DRC command to check the distance between the N+ diffusion regions of different potentials so that ESD failure is prevented e effectively. TLP current pulse signal is added to the drain of the GGNMOS device, at the same time the gate, source and substrate of it are grounded. As the result, the V_D - I_D characteristic coincides with the snapback obtained by theoretical analysis after GGNMOS layout optimization.

7 Relation to prior work

Recently a LDO (Low Dropout Linear Regulator) layout of SOC is designed based on 0.13μm. The ESD protective device is using the GGNMOS designed according to this work. At last we will research for ESD characteristics biased on nan-meter process.

Acknowledgment

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