Research on data transmission application based on USB3.0 bridge chip and FPGA

Dezhuang Ma*, and Lunhui Deng

Communication University of China, Beijing 100020, China

Abstract. Aiming at the shortcomings of data transmission system, such as poor portability, unstable data transmission and high cost, the combination of FPGA and USB3.0 technology is adopted to realize the real-time and reliable access to the host computer platform. Practical application shows that this platform has the advantages of small size, low power consumption, hot plug, etc. And the system meets the design requirements.

1 Introduction

Over the past years, Digital Signal Processing (DSP) technology has been widely applied in a variety of real-world applications, such as communications, image, aerospace, medical and other fields. FPGA has an increasingly wider application in digital signal processing because of its advantages in high level of integration, high speed, and programmability. Usually the signal processed will be sent to PC for further display and processing. However, the difficulty is that there is no dedicated communication interface between FPGA and PC. It is known that Universal Serial Bus(USB) has a high transmission speed, hot plugging, portability, simple interface etc [1]. Therefore this paper achieves data transmission with the use of FTDI FT601Q - USB3.0 to FIFO bridge chip. Experiments show that this system can achieve real-time data transmission from the external world by FPGA to PC side.

2 Requirement analysis

In order to meet the needs of data transmission, considering objective factors such as cost, power consumption, volume and others, this paper selected Altera's FPGA, FTDI's FT601Q chip. The data transmission system is divided into three parts:

- The data is written by the external world to FPGA's FIFO buffer.
- The data is written by FPGA to FT601 bridge chip FIFO.
- The data is transmitted by FT601 FIFO to the host computer [2].

In order to achieve the correct transmission of data, the system must meet the following aspects:

First, the host computer can get the information of FT601Q bridge chip and data from FT601Q bridge chip. Second, the read and write timing of FT601 must be set correctly, ensuring data can be written correctly by FPGA. Third, FPGA should have buffers for data

* Corresponding author: mdz800@cuc.edu.cn

staging to achieve the purpose of external data writing without interruption and loss. Finally, the system can be self-checked.

3 System design

Figure 1 shows major blocks of the data transmission system. The main function that the systems should achieve is to transfer the data from the outside to the host computer through FT601Q. In the process of data transmission, external data should be designed as regular, and then sent to FPGA FIFO. After detecting the enable signal from FT601, FPGA control center began to read and write data to FT601. And in the end, host computer get the data from FT601 through the extension wire of USB 3.0. By comparing the similarities and differences between the data received in the PC computer's memory and external data, the reliability of the system can be checked.

Fig. 1. Structure diagram of system.

The selected FPGA 5CEFA5F23I7N of this design is Altera's Cyclone V FPGAs. The devices are built on TSMC's 28nm Low-Power (28LP) process, which brings down the power and cost required by cost-sensitive applications. Based on the simplicity of the system, FPGA FIFO calls Altera IP core. FT601Q supports super speed (5Gbps), USB High speed (480Mbps) and USB2.0 Full speed (12Mbps) transfer. And FT601Q supports 2 parallel slave FIFO bus protocols, Multi-Channel FIFO mode Protocols and 245 Synchronous FIFO mode Protocols. The chip has buffers with 16k bytes, supporting large data bursting.

3.1 Operation Principle of FT601

Chip uses 245 Synchronous FIFO mode Protocols. This slave bus uses one IN and one OUT FIFO channel while in this mode. TXE_N is an output signal, Transmit FIFO empty. It is active low and when active it indicates the Transmit FIFO has space and is ready to receive data from the FIFO master. And the master has write cycle when WR_N is driven low by the bus master. BE [3:0] is byte enable signal. In bus master write operation, the bus master asserts the signal for the valid bytes in a word strobe. When the FT601 FIFO is full, that is, when the amount of data written is 4KB, the host will read the data in the FT601 FIFO into memory. Subsequently, the next data transfer begins. The data from the PC to FPGA is similar to the above process, but in the opposite direction [3].

Figure 2 shows 245 Synchronous FIFO mode bus master write cycle.

Fig. 2. 245 Synchronous FIFO mode bus master write cycle.

3.2 Firmware Program’s Design Of FT601

Firmware program’s design of FT601 is designed mostly for read and write state machine. It describes the communication between the USB chip and FPGA. It mainly consists of four states: Initial wait state-SIDLE, Bus master read state-SRddb, Bus master write state-SWRdb, Read and Write completion state-SSTOP [4].

Figure 3 shows Firmware logic state machine of FT601.

Fig. 3. 245 Synchronous FIFO mode bus master write cycle.

3.3 Interface Design Of FPGA FIFO

FPGA FIFO is a buffer for data staging to achieve the purpose of external data writing without interruption and loss. DDR has the advantage of large capacity and fast transmission speed, but high hardware complexity and high cost. Instead of DDR, the system uses Altera IP core, which has a bit width of 32bits, a depth of 65536 words. When FT601 is ready, the FIFO of FPGA starts writing data, and when the data is greater than 4KB and the FT601 can receive data, the data is written from FPGA to FT601 [5].

3.4 Design Of PC Software

FTDI provides FT601 chip driver, as well as the corresponding application program interface. System uses Visual Stdio 2015 to write PC software, enabling communication between PC and hardware. System uses FT60X Configuration Programmer User Guide and FT600ChipConfigurationProg.exe to enable the chip operating mode settings [6].

4 PERFORMANCE EVALUATION

4.1 Test Environment

Table 1 shows the test environment of system.

Table 1. Test environment of System.

Project	Description
Date Operating system	Windows10 Professional 64bit
CPU	Intel(R) i7-6700 3.40GHz
Memory	4GB
USB chip model	FT600Q (USB3.0 to FIFO Bridge)
SoftWare	Microsoft Visual Stdio 2015 ModelSim-Altera 10.1d (Quartus II 13.1)

4.2 Read and Write test of FPGA FIFO

The purpose of this part is to test whether external data can be exported correctly through FPGA FIFO. The test tool is ModelSim, which writes an appropriate Testbench. Input data changes circularly from 0 to 1023.

Figure 4 shows the simulation chart of FPGA FIFO. It can be seen from the figure that when the data of FPGA FIFO reaches 4KB, the data is read correctly from FPGA FIFO.

Fig. 4. Simulation chart of FPGA FIFO.

4.3 Read and Write test of FT601 FIFO

There will be data loss when external data directly transmit into FT601 and then to PC. The purpose of this part is to test the speed of data transmission and the timing validity. The correctness of the data transmission is verified when the system is tested as a whole.

Apply 100 blocks memory on PC to access data, each of which is 63Mbit. System uses the memory space cycle coverage method to realize data uninterrupted transmission. According to data sheet, FT601x data bursting rate is up to 400Mbyte/s. In actual test, FT601 burst read and write at a rate of about 378Mbyte/s, regardless of read-write interval. With the size of the transmission data flow, the PC burst reading interval is not the same. The data transmission flow of the system is 63Mbit. Using the API functions QueryPerformanceFrequency and QueryPerformanceCounter provided by the Windows system can achieve high precision timing of data transmission. After several measurements, the average transmission time of 100×63Mbit data is 2.485 seconds, and the transmission speed is approximately 317Mbyte/s.

Figure 5 shows the SignalTap screenshot of bus master write timing.

Fig. 5. SignalTap screenshot of bus master write timing.

4.4 Overall Functional Testing Of The System

The purpose of this section is to verify the correctness of the overall system function, including the correctness and speed of data transmission. The test input data is 0 to 26843545559, changes with a 1 cycle interval. The test input data is first written to FPGA FIFO, and then passes through FT601, before transmission to PC. PC will check the data received in memory, using the regularity of test input data.

The overall system performance verification mainly consists of two parts: First, it should be checked that if FPGA FIFO had 'full' status during the transmission of the data. If so, this will cause interruption of external data transmission, resulting in data loss. Second, verify that the data received by the PC is consistent with the outside data.

After verification, the system began to work normally after no more than 0.05 seconds of instability. When the system is stable, the maximum real-time transmission speed of data is 118Mbyte/s. The reason for the low data transmission speed is that the FPGA FIFO is only 2Mbit. It is known from section C, chapter IV that the above test speed can reach 317Mbyte/s when FPGA selects a larger FIFO.

5 Conclusion

The design uses Altera Cyclone V 5CEFA5F23I7N and FTDI FT601Q-USB3.0 to FIFO bridge chip to realize a data transmission system. The system can transmit data in real time from the external to PC. By setting up platform, the debugging of hardware and software is realized, and the feasibility and stability of the system are proved. In addition, this design proves that the transmission speed can be further improved with the increase of hardware cost.

References

1. Kuang Peng, Liu hong, Wang YongGang. Design of Universal Data Transmission System on FPGA and USB3.0 [J]. *Microcomputer and Application*. 2017, 36(7); 26-28, 34.
2. Zhang HuiXin, Shi YongLiang, QINLi,CUI JianLi. The Application of USB3.0 Interface in Sub Data Storage System. *Computer Measurement and Control*. 2015.23 (3).
3. FT600Q-FT601Q IC DatasheetDatasheet Version 1.02.
4. Luo Jun, Du Jiechu. USB Protol and Its Implement of USB Interface. *Chinese Journal of Scientific Instrument*. Vol. **25** No.4. Aug, 2004.
5. Zhang YaoZheng, Wang WenLian, Zhang ZhiJie. Study on multi-channel synchronization acquisition and storage system based on one FIFO. *Power System Protection and Control*. Vol. **38** No.8. Apr.16, 2010.
6. Pei XiangDong, Chen Xiao, Tan QiuLin, Zhang ZhiJie, Xiong JiJun. Design of Communication Between PC and FPGA Based on USB—FIFO. *Computer Measure & Control*. 1671-4598 (2012) 04-1073-03