Hardware Platform Design for Baseband Data Transmission of WCDMA Based on USB3.0

Fu Xiao[1,2] and Xiao Li-ming[1]

[1]Department of Electronic Engineering, Tsinghua University, Beijing, China
[2]Innovem Technology (Tianjin) Co., Ltd, Tianjing, China

Abstract: This paper proposes a hardware platform for WCDMA baseband data transmission, which consists of USB3.0 interface, general purposes processor (GPP), and software defined radio (SDR) system. In view of the requirements of WCDMA system, the hardware platform consisting of USB3.0 controller, FPGA and DDRII was selected, which finally realized the high throughput rate and low delay transmission of baseband data of WCDMA system. The experimental results show that in this GPP software defined radio system, the interface speed of USB3.0 can reach 200MBps, and the loopback delay time of the system is about 0.7ms, which can meet the requirements of WCDMA system.

1 Introduction

WCDMA[1] is one of the third-generation wireless communication standards adopted by the International Telecommunication Union (ITU). It adopts Frequency Division Duplex (FDD), which has the advantages of flexible service, high spectrum efficiency, wide capacity and wide coverage.

Software defined radio (SDR)[2] is an architecture of a wireless communication system proposed in the 1990s. It has the advantages of short development cycle, high efficiency, low cost, and flexibility, and is suitable for forward-looking research. At work, the main software defined radio platforms currently include general purpose processors (GPP), FPGA, and DSP. FPGA can process data in parallel, DSP has powerful digital signal processing capabilities, so they are widely used in software defined radio, but FPGA and DSP programming and debugging have high requirements for developers[3]. In recent years, with the continuous improvement of the performance of GPP, the application of GPP in software defined radio systems has become more and more extensive. In this paper, software defined radio systems based on GPP and Windows operating systems are mainly discussed.

2 WCDMA system requirements and analysis

2.1 WCDMA system bandwidth requirements

Before designing the hardware platform, we need to know the amount of data transmitted by the WCDMA system and its bandwidth. The WCDMA system uses 10ms as a frame. Each frame consists of five 2ms subframes. Each frame can be divided into 15 time slots. Each time slot has 2560 chips. That is 3.84M chips per second[4], its frame structure is shown as in Fig. 1. According to the Nyquist sampling theorem, for the distortion-free recovery signal, the sampling frequency of the system must be twice the signal bandwidth. On the other hand, in order to obtain a higher signal-to-noise ratio when performing baseband signal extraction, we will The sampling frequency of the downlink channel is set to be 4 times of the system chip rate, that is, 3.84 Mcps × 4 = 15.36 Mcps. For each sample, Three bytes are used for quantization, and the data amount of the downlink channel for one second is 15.36 Mcps × 3 Bytes = 46.08 × Bytes. The data amount of each 2ms downlink subframe is: 46.08×10^6 Bytes / (500 × 1024) = 90KBytes. For the uplink channel, no oversampling is performed, the clock is sampled using 3.84M, and then quantized by 3 Bytes, the data amount of the uplink one second is 3.84Mcps×3Bytes=11.52×Bytes, and the data of each 2ms uplink subframe The amount is: 11.52×10^6 Bytes / (500 × 1024) = 22.5KBytes. Therefore, the amount of data per uplink subframe is 22.5 KBytes. The working mode of the WCDMA system is Frequency Division Duplex (FDD), so the data of the uplink and downlink channels need to be transmitted at the same time, so the bandwidth requirement of the WCDMA system at the above sampling rate is: 46.08MBps+11.52MBps=57.6 MBps = 460.8 Mbps.

[a] Corresponding author: author@e-mail.org

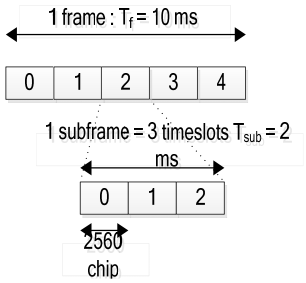

Figure 1 Frame structure of WCDMA system

2.2 WCDMA system delay requirements

In order to implement baseband data transmission for WCDMA systems on a hardware platform, we need to meet all the requirements mentioned in the chapter 1. This paper takes the HARQ of WCDMA terminal system as an example. In the WCDMA protocol, the HARQ response information of one downlink subframe should be placed in the uplink subframe after it is received for 5 ms, and the HARQ response time of the WCDMA system is as shown in FIG. 2. After receiving a downlink subframe in position 1, the HARQ ACK/NAK feedback must be in the uplink subframe after 5 ms, that is, in the uplink subframe after position 2 (the dark color in the figure is a downlink subframe). The frame and the corresponding uplink subframe carrying the HARQ feedback information). The time between the 1st position and the 2nd position is 5ms.

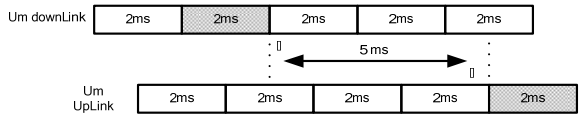

Figure 2 HARQ response diagram of WCDMA system

3 Hardware platform design

According to demand, a baseband data transmission system composed of USB3.0 controller and FPGA is adopted, and its structure is shown in Fig. 4. As the core of the control, the FPGA completes the operation of collecting data from the RF end and sending it to the USB 3.0 controller and collecting data from the USB 3.0 controller to the RF end. The USB3.0 controller mainly completes the USB3.0 protocol for communication between the GPP and the hardware platform and the data transmission based on the USB3.0 protocol. To meet this requirement, a USB3.0 controller peripheral chip is used in the design. CYUSB3014[5], which introduces the ARM9 processor as the core, internally uses the AHB bus mode, loads the ThreadX operating system, and implements the USB3.0 communication protocol and is backward compatible with USB2.0 and USB1.0 communication. Protocol, its interface with the FPGA is a programmable Slave FIFO interface[6], the interface's maximum operating frequency is 100MHz, can support up to 32bit parallel data transmission, therefore, the interface can reach 3.2Gbps transmission rate. This interface is a bidirectional multiplexed port, that is, the "read" and "write" operations can only perform time division operations. In terms of caching, two 1Gbit DDRII memories are added to the hardware platform during design. The frequency of the interface can reach the maximum operating frequency of FPGA of 166.7MHZ, and the maximum transmission rate in reading and writing memory can reach 5.3Gbps. Since the transmission rates of the three parts of the USB 3.0 controller, the DDRII memory, and the RF interface are different, a FIFO is added between them to change the rate. This module does not affect the transmission rate of the hardware platform. In summary, we can find that the interface rate between FPGA and USB3.0 controller, DDRII and RF terminal is constant, so the speed at which USB3.0 controller communicates with GPP determines the transmission rate of hardware platform.

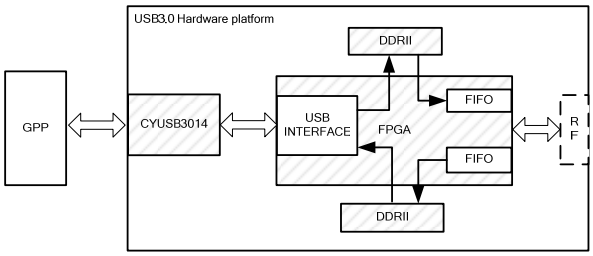

Figure 3 Hardware platform system structure diagram

4 Hardware platform performance analysis

4.1 System transmission rate analysis

In order to ensure the correctness of data transmission, the block transmission mode is used as a method for data transmission between the USB 3.0 controller and the GPP in the design, and the packet length is 1 Kbyte. In the communication mode, USB3.0 adopts full-duplex communication mode, so USB3.0 adds “burst” operation to Endpoint in the feedback mechanism, that is, Device or host does not receive confirmation information, Can continue to transfer a certain number of packets, each packet size is 1KByte. The longer the "burst" length, the higher the transfer rate is. The CYUSB3014 can support up to 16 bursts. In the experiment, the maximum burst that the USB3.0 controller can support is set to 16. In addition to the "burst" length will affect the system's transmission rate. the size of the internal Buffer of the USB3.0 controller will also affect the rate of transmission.

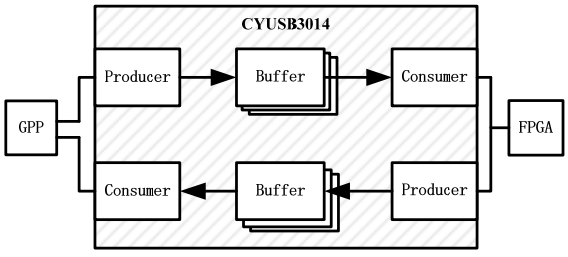

Figure 4 CYUSB3014 internal transmission structure diagram

the DMA mechanism[7] is adopted inside the USB3.0 controller CYUSB3014, and two transmission channels are established. The internal structure is shown in Figure

4, which can be seen from the figure. There are multiple Buffers in the channel to buffer the data. The internal transmission is based on the Buffer. When a Buffer is filled by the Producer, the CYUSB3014 will generate a response message to inform the Consumer to read the data from the Buffer for transmission. The Buffer size is different, the amount of data transmitted each time is different, and the transmission rate will be different.

In the experiment, the effect of Buffer size on the transmission rate was tested, and the result shown in Fig. 5 was obtained. It can be seen from the figure that the transmission rate is positively correlated with the size of the Buffer, and the larger the Buffer is, the transmission rate is The higher. The size of the Buffer needs to be set according to the requirements of the system. For the sake of implementation, the data volume of one sub-frame is preferably divisible by the Buffer. Since the requirement of the WCDMA system for the hardware platform is a real-time transmission system, the data transmission delay cannot be greatly offset, and the hardware platform has better performance. As can be seen from Section 2, the data volume of one downlink subframe is 90KByte, so the size of the Buffer can be set to 6KByte. At this time, the data of one downlink subframe is divided into 15 transmissions, and the transmission rate of USB3.0 under this condition. At 200MBps, it can fully meet the requirements of the system from the perspective of throughput. In the following, I will discuss whether the WCDMA system can meet the transmission delay time requirements at this rate.

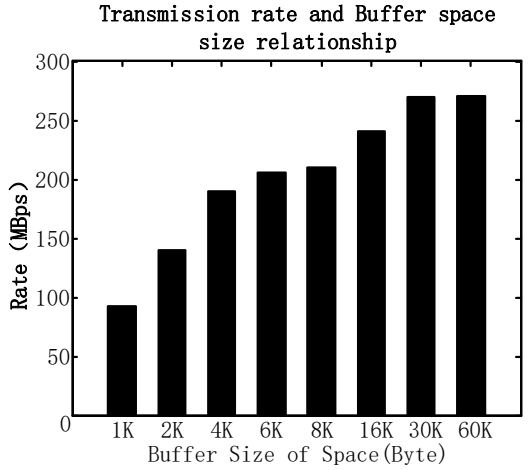

Figure 5 CYUSB3014 internal transmission structure diagram

4.2 Loopback delay analysis

In the previous section, you can see that the transfer rate of USB3.0 on the hardware platform is proportional to the size of the Buffer, and the Buffer size will be measured in the actual test on the premise that the data amount of one sub-frame can be divisible by the Buffer. Buffer size is set to 6Kbyte. In order to give the GPP more processing time, in the case that the system performance can be satisfied, we set the time for the GPP to send the uplink subframe to receive the first 18KByte data of one downlink subframe, so that the GPP end pairs each downlink. Sub-frame baseband sampling data reception is divided into two parts, the first part is 18Kbyte, and the second part is 72Kbyte. The process of HARQ for a WCDMA system is simulated in Figure 7 by means of data transmission. If a subframe starts to be received by the hardware platform at position 1, the corresponding HARQ feedback information should be sent to the air interface in the uplink subframe at position 2. The time of the portion 5 in Fig. 6 is the time of the GPP processing.

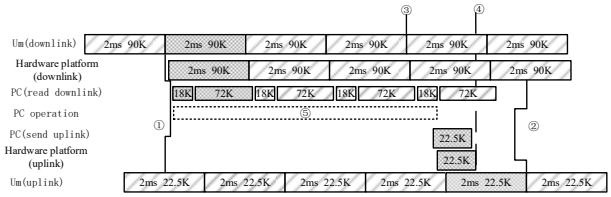

Figure 6 WCDMA system data flow chart

In order to intuitively reflect the delay time of the hardware platform, the design time is removed from the GPP processing time, so the starting point of the timing is selected at point 3 in Figure 6, and the end point of the timing is the 4th point, that is, the hardware platform receives the uplink. After one frame of data, the time calculated at this time is the time consumed on the hardware platform. We call this part of the time "loopback delay time". Since the transmission rate of USB 3.0 is affected by the bandwidth of the USB on the GPP, the usage of the GPP core, and the like, the time for data to be transmitted from the hardware platform to the GPP memory is an indefinite value. As can be seen from Fig. 7, starting from the timing point 3, the data of the uplink subframe needs to be transmitted within 3 ms (that is, the position of the 4th point must be in front of the 2nd position), otherwise the data of one uplink subframe is The transmission cannot be completed on time, causing uplink packet loss.

In the design, we choose the desktop computer with the USB3.0 interface for testing. The results of the test are shown in Figure 7. The abscissa is the time of the delay and the ordinate is the probability distribution of the loopback delay time.

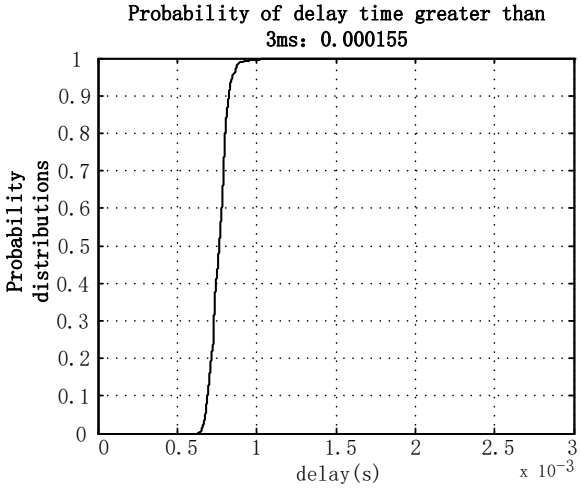

Figure 7 WCDMA system loopback delay time distribution

It can be seen from the test results that the loopback delay time is mainly concentrated between 0.6 and 1 ms, and GPP has ample time to process the data. It can be seen from the statistics in Fig. 7 that the probability of

delay time greater than 3ms is 1.55×10^{-4}. And the requirement of the WCDMA system for the air interface packet loss rate is 10^{-3}. That means the packet loss rate due to the delay of the hardware platform is much smaller than the packet loss rate of Um. So this hardware platform can meet the requirements of the WCDMA system. To meet higher latency requirements, you can choose a Windows-based real-time operating system, such as IntervalZero[8], which is to be continued in future research.

5 Conclusion

In this paper, we analyze the feasibility of applying USB3.0 technology to GPP-based software defined radio system, and realize the high-speed transmission of baseband data of WCDMA system through hardware platform with USB3.0 controller and FPGA. Through analysis and experiment, the maximum transmission rate of USB3.0 can reach 260MBps under the hardware platform framework of this paper. The highest transmission rate for WCDMA system can reach 200MBps, and the loopback delay time is about 0.7ms. The result proves that with USB3.0 technology, the bandwidth and delay requirements of the WCDMA system in the baseband data transmission can be met on the GPP software defined radio system.

References

1. 3GPP TS 25.201 V10.0.0. Physical channels and mapping of transport channels onto physical channels (FDD) [S].2010.
2. P. Johnson.New Research Lab Leads to Unique Radio Receiver[J]. E-Systems Team, May 1985, Vol. 5, No. 4, pp 6-7.
3. P. Pawłowski, A. Dąbrowski, P. Skrzypek. Software defined radio - design and implementation of complete platform[C]. IEEE 14th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Cottbus,2011.
4. 3GPP TS 25.211 V10.0.0. Physical channels and mapping of transport channels onto physical channels (FDD) [S].2010.
5. Cypress Semiconductor.EZ-USB® FX3 SuperSpeed USB Controller[S].2012.
6. Cypress Semiconductor. Designing with the EZ-USB® FX3 Slave FIFO Interface[S].2012.
7. Cypress Semiconductor.FX3 Programmers Manual[S].2012.
8. IntervalZero RTX RTOS[OL], www.intervalzero.com.