

# Nondestructive testing method for a new generation of electronics

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**Abstract** The implementation of the Smart City system needs reliable and smoothly operating electronic equipment. The study is aimed at developing a nondestructive testing method for electronic equipment and its components. This method can be used to identify critical design defects of printed circuit boards (PCB) and to predict their service life, taking into account the nature of probable operating loads. The study uses an acoustic emission method to identify and localize critical design defects of printed circuit boards. Geometric dimensions of detected critical defects can be determined by the X-ray tomography method. Based on the results of the study, a method combining acoustic emission and X-ray tomography was developed for nondestructive testing of printed circuit boards. The stress-strain state of solder joints containing detected defects was analyzed. This paper gives an example of using the developed method for estimating the degree of damage to joints between PCB components and predicting the service life of the entire PCB.

## 1. Introduction

The Smart City is the latest development in the field of urban planning. The key resources for implementing the Smart City strategy are information and intelligent processing systems designed to ensure a stable link between individuals and knowledge. This will become the driving force for the transition to a fundamentally new way of energy consumption [1]. The Smart City system integrates all information flow into a single center where data is accumulated, systematized and processed. The operational performance of this analytical center depends on smooth operations of all computer systems and servers. Since electronic devices and their components are becoming more and more compact, new nondestructive testing methods need to be developed.

Two nondestructive testing methods, optoelectrical and X-ray, are widely used to control the quality of electronic products [2, 3]. Optoelectrical systems can be used to monitor and analyze performance of automatic installation equipment and to measure qualitative parameters of solder joints. These systems, however, do not guarantee the

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detection of latent defects (hidden defects that have not been detected through standard tests of printed circuit boards (PCB) but can lead to PCB failure during operation).

At present, the X-ray method allows us to test a PCB with a resolution of 0.5  $\mu\text{m}$ , to identify all discontinuities in its design, and to create a detailed 3D model of the test object. This analysis requires significant time and additional risk assessment of identified defects. With these methods, it is difficult to identify latent defects that will be growing in size during the operation of a device with PCB. This makes it impossible to accurately predict the service life of the entire device.

The analysis of the existing nondestructive testing methods demonstrates that the acoustic emission (AE) method can be adapted to identify growing design defects of printed circuit boards. Mistras, (USA), is one of the companies engaged in research in this field. The researchers detected latent defects in printed circuit boards with BGA chips. The defect localization accuracy was within a circle with a radius of 1 mm [4–6].

Based on the results of theoretical and experimental studies performed by the authors, the difficulty in using the AE method for defect identification in PCB can be explained by the following reasons. Firstly, solder joints (test object) have small geometric dimensions (on the surface of a 40 x 40 mm chip, there are from 600 to 1,200 solder joints). Secondly, the PCB design combines four materials with different technical characteristics (ceramics, copper, solder, and fiberglass).

The experimental studies on sample PCBs show that the AE method can detect a growing design defect of a PCB (the probability of defect detection is 85%). However, it is difficult to determine defect criticality in areas with high packing density on the basis of AE data [7].

In order to clarify the location of latent defects and determine their geometric dimensions through numerical analysis, the authors suggest combining the acoustic emission method with the X-ray tomography method. This study is the first to use such an integrated nondestructive testing approach to printed circuit boards.

## **2. Materials and Methods**

Mechanical characteristics of the POS-61 solder material designed to attach a chip to a PCB were determined using the INSTRON 8801 (USA) fatigue testing system. The tests were carried out in compliance with GOST 1497-84 [8].

Cyclic tests of the POS-61 solder material were performed using the INSTRON 8801 fatigue test system (USA). The tests were carried out in compliance with GOST 25502-79 [9].

In order to localize latent design defects of a PCB, the AEWIn software and Micro2 digital AE system (USA) were used [10].

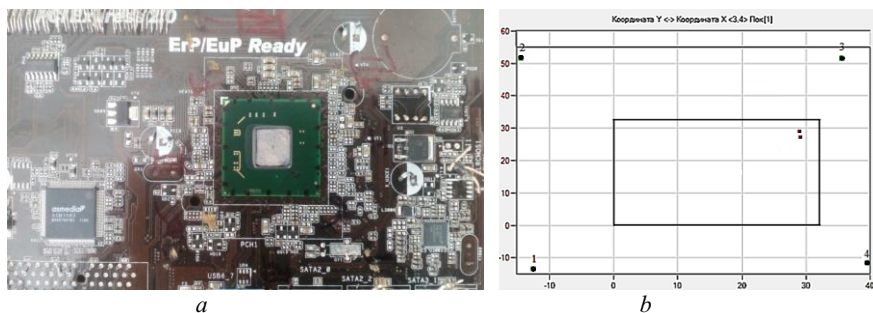
Geometric dimensions of detected latent defects were determined by a Y. Cheetah 160kV microfocus X-ray inspection system [11].

In order to determine the maximum stress rate in the solder material under a given load, BGA solder joints were numerically modeled using the ANSYS Mechanical software package.

## **3. Experiment**

### **3.1 Identification of Latent Design Defects in a Printed Circuit Board Using the Acoustic Emission Method**

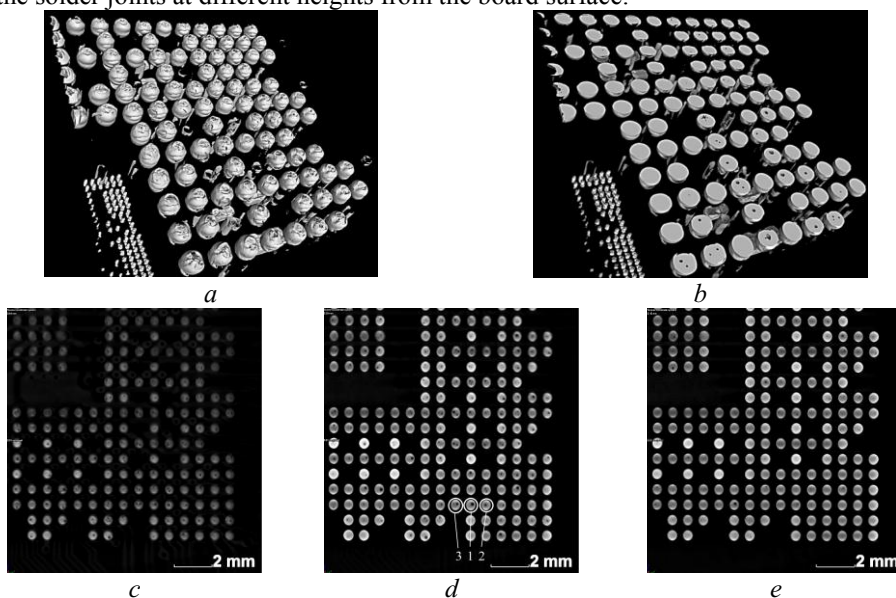
A video card containing a BGA chip on its surface was selected as a sample printed circuit board for the experiment. The geometric dimensions of the chip package are 0.032 x 0.032 m. It is located in the center of the video card (dimensions of the PCB: 0.07 x 0.14 m). The sample printed circuit board is shown in Figure 1a. Defects were found using a planar location test setup with four sensors. A diagram in Figure 1b shows the results of defect identification (in the figure, ● means the AE sensor; ■ means the detected defect). In the diagram, the locations of sensors are indicated by numbers. The chip boundaries are shown by rectangular outline. The test results demonstrate that there are “active” defects in the top right corner of the chip that can lead to failure of the PCB during its operation.



**Fig. 1.** AE tests: a – sample PCB; b – diagram of defect identification results.

### 3.2 Determining Geometric Dimensions of PCB Latent Defects

In order to determine the geometric dimensions of detected growing defects, the PCB was tested by using a Y. Cheetah 160kV microfocus X-ray inspection system. The experimental results are given in Figure 2. Figure 2a presents a 3D reconstruction of solder joints through which geometric dimensions of any defects can be determined. Figure 2b–e shows sections of the solder joints at different heights from the board surface.



**Fig. 2.** Experimental results: a – 3D reconstruction of solder joints, b – section of solder joints, c – 0.37 mm, d – 0.20 mm, e – 0.06 mm.

Thus, by combining AE and X-ray tomography methods, it is possible to determine the geometry of a growing defect. The service life of the PCB can be determined by numerically analyzing the stress-strain state of solder joints under operating loads.

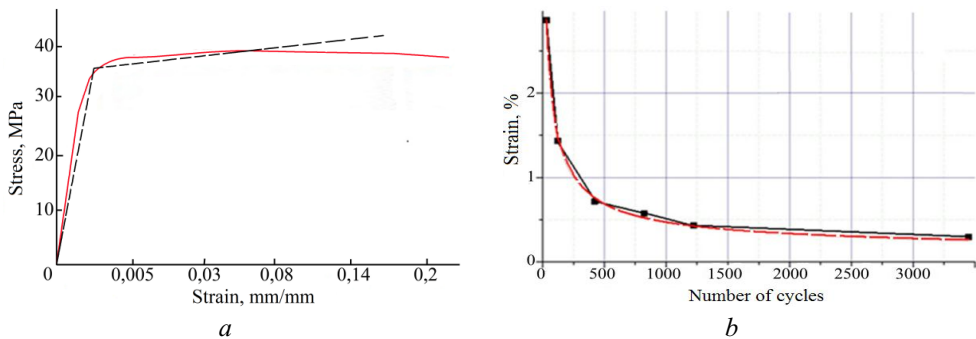
### 3.3 Numerical Analysis

#### 3.3.1 Determining Mechanical Characteristics of POS-61 Solder Material

Uniaxial tensile and cyclic tests were carried out to determine mechanical characteristics of the solder. Based on the results of uniaxial tensile tests, the bilinear stress-strain curve for the solder material (the solid and dashed lines represent the experimental data and the bilinear approximation, respectively) (Fig. 3a). Parameters of the long-term strength model were determined on the basis of the Manson-Coffin equation:

$$N^m \Delta \varepsilon = C_N, \tag{1}$$

where  $N$  is the number of cycles for a given deformation;  $\Delta \varepsilon$  is the strain range;  $C_N$ ,  $m$  are parameters of the model (for this material  $C_N = 0.1892$ ,  $m = 0.53$ ). The results of theoretical calculations (dashed line) and experimental data (solid line) are reconciled in Figure 1b.



**Fig. 3.** Test results: *a* is the stress-strain behavior in the sample; *b* is the dependence of strain rate on the number of cycles prior to fracture.

#### 3.3.2 Damage Rate Function of the Material

To determine the current state of the material and predict the remaining service life, let us introduce the damage rate function proposed by V.V. Moskvitin [12] that must satisfy the following conditions:

$$\omega(0)=0, \quad \omega(t^*)=1, \tag{2}$$

where  $t^*$  is the time prior to the limit state (fracture).

The following expression can be introduced to assess the degree of material damage:

$$\omega(t, T) = \int_0^t \frac{(1 + m_1)(t - \tau)^{m_1}}{t_0(\varepsilon, T)^{1+m_1}} d\tau, \tag{3}$$

where  $m_1 = -1 + 1/m$  (for the solder material  $m = 0.53$ );  $\varepsilon$  is the strain rate;  $t_0$  is the durability of a given material determined experimentally at temperature  $T$  and not

depending on deformation time. Let us use a special case to estimate the degree of damage of solder joints exposed to thermal cycling (3):

$$\omega(t, T) = \nu \int_0^t \frac{(1 + m_1)(t - \tau)^{m_1}}{[C_1(a - bT)\Delta\varepsilon^{-m}]^{1+m_1}} d\tau, \tag{4}$$

where  $\Delta\varepsilon$  is the time-independent strain range;  $\nu$  is the loading rate,  $C_1$  and  $m$  are, respectively, the parameters of the model determined for this material, where  $C_N(T) = C_1 \cdot E(T)$  and  $E(T) = a - bT$  ( $C_N = 18.92$ ,  $m = 0.53$  at  $25^\circ\text{C}$ );  $a$  and  $b$  are the parameters of the model that show the temperature's dependence of the material's elastic modulus ( $a = 6.4411$ ,  $b = 0.0284$ ).

After integrating the relation (4), we obtain an analytical dependence of material damage on time and at a given temperature  $T$  different from the initial one:

$$\omega(t, T) = \left[ \frac{\nu}{C_1(a - bT)} \right]^{\frac{1}{m}} \Delta\varepsilon t^{\frac{1}{m}} \tag{5}$$

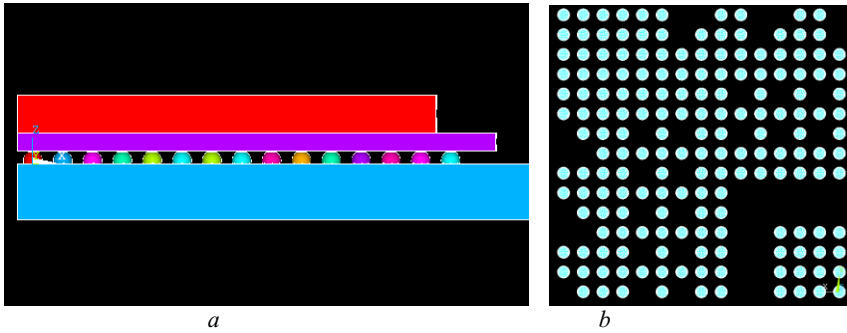
### 3.3.3 Estimating the Load-Bearing Capacity of Solder Joints

In order to predict the service life of a printed circuit board with detected defects, it is necessary to assess the stress-strain state of defective solder joints by means of numerical analysis. In our problem, we determined the stress-strain state of the printed circuit board at a temperature cycle from  $-55$  to  $+85^\circ\text{C}$  by exposing it to the maximum and minimum temperatures for 20 minutes. The rate of cooling and heating was  $10^\circ\text{C}/\text{min}$  [13].

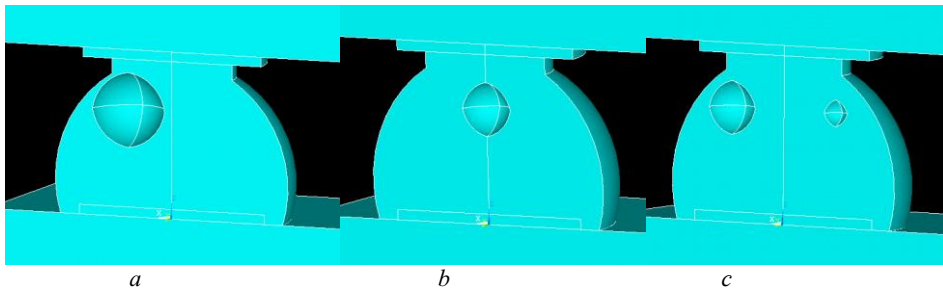
In order to take into account all boundary conditions and loads to which the solder joint is exposed during thermal cycling, it is necessary to consider two types of numerical models: general and local ones [14].

The general model represents the entire printed circuit board (Fig. 4). The model contains a printed circuit board, contact pads on a printed circuit board and on a chip substrate, a substrate, a chip, and a ball grid array. Since the problem is axisymmetric,  $\frac{1}{4}$  of the printed circuit board design is considered. The result of the solution is a displacement field for all model nodes. Next, this displacement field is applied to solder joints that have defects in the local model in order to determine the maximum stress rate.

The local model represents a defective solder joint. Three cases of defective contacts are considered (Fig. 5 and Fig. 2d). The model contains a printed circuit board, contact pads on a printed circuit board and on a chip substrate, a substrate, and a solder joint. The data obtained in the general model are used as a load in the local model. Since the problem is axisymmetric,  $\frac{1}{2}$  of the solder joint design is considered.



**Fig. 4.** Global model: *a* is the general form; *b* is the BGA.



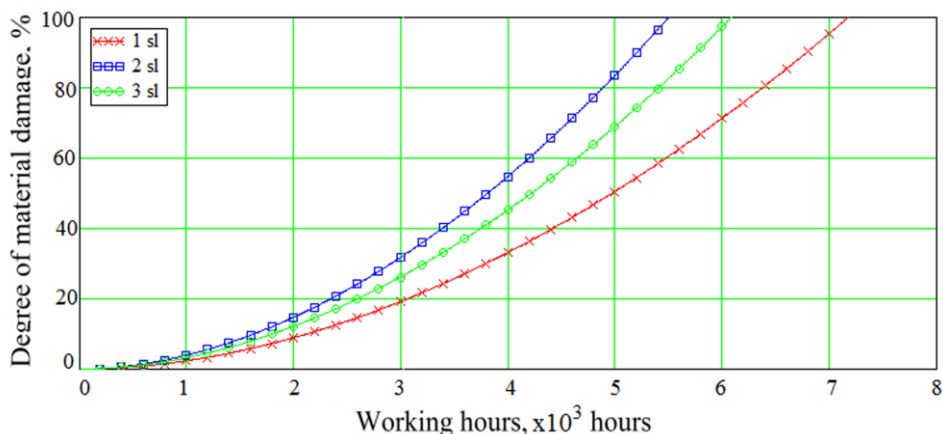
**Fig. 5.** Local model: *a* is the first; *b* is the second; *c* is the third cases.

Based on the results of numerical simulation, maximum stress rates were determined in each of the considered cases: 1 –  $1.86 \cdot 10^7$  Pa; 2 –  $3.07 \cdot 10^7$  Pa; 3 –  $2.53 \cdot 10^7$  Pa. Shear strain can be calculated from the ratio (its form was determined from uniaxial tensile tests of solder samples):

$$\varepsilon(\sigma, t) = \left( \frac{\sigma}{E} \right) + A_1 \left( \frac{\sigma}{E} \right)^{B_1}, \text{ where } A_1 = 1.17 \cdot 10^{57}, B_1 = 22.26, E = 16.082 \cdot 10^9 \text{ Pa.}$$

In order to determine the number of cycles until the solder joint loses its load-bearing capacity under a given load (the duration of the temperature cycle is 68 min, the loading rate  $v = 2.45 \cdot 10^{-4}$  cycles/s), the expression (5) is used.

Based on the results of the solution, we determined the degree of damage as a function of the operating time at a given loading rate for each case of a defective solder joint (Fig. 6). The curve shows that, at a given loading rate, the defective solder joint of the second case has the shortest time of failure. In this case, the service life of the PCB is 5,500 hours.



**Fig. 6.** The damage accumulation function for the three considered cases of damaged joints.

## 4. Results

By combining AE and X-ray tomography methods, we localized growing defects and determined their geometric dimensions. Using the developed numerical modeling algorithms and methods aimed at predicting the remaining service life based on loading history of the PCB, we predicted the service life of the PCB under given operating loads.

## 5. Conclusion

Based on the results of the studies, a nondestructive testing method for electronic equipment was developed. Using this method, it is possible to identify latent design defects of PCB, to analyze their criticality, and to determine the residual service life of PCB. The method can be used in the production of printed circuit boards and the testing of new solutions before commercialization. The method is also applicable to estimating the service life of equipment during operation. This innovation is necessary for the reliable functioning of Smart City systems.

The application of the developed method was demonstrated for PCBs containing BGA chips. Further research should be devoted to justifying the general applicability of this method to printed circuit boards of any configuration.

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