

A High Efficiency RF Power Amplifier Using Linearity-Enhanced Method in 40nm Standard CMOS Process

Wang Cheng¹, Ting-Ting Mo*

¹ Center for Analog/RF Integrated Circuits (CARFIC)
School of Electronic Information and Electrical Engineering,
Shanghai Jiao Tong University, Shanghai 200240, China
* Email: wangcheng1992@sjtu.edu.cn

Abstract. A two-stage RF CMOS power amplifier with high linearity for WLAN is presented in this paper. The proposed PA consists of a programmable gain amplifier and a high power stage which is composed of a main amplifier with class AB bias and an auxiliary amplifier with class C bias. To improve the linearity, an integrated diode linearization circuit provides a compensation mechanism for the input capacitance variation of the active devices, improving the linearity from the gain compressing. Moreover, based on the un-even bias scheme, the power stage can improve linearity and reduce current consumption in the low power region. In order to demonstrate the feasibility of the technique, two types of PAs have been designed. The improved PA at 3.3V supply voltage, has a 37dB of power gain, 1.1 dBm increase of P, 8.3% increase of PAE@P and dB increase of ACPR for 802.11g WLAN, respectively, as compared with the traditional PA.

1. Introduction

Due to low cost and ease of integration complementary metal oxide semiconductor (COMS) is becoming the technology of choice for most wireless application. The past few years have seen a lot of advancement in CMOS circuit design as well as device technology, which have made it possible to implement RF circuit blocks in CMOS with performance just as good as any other technology. RF blocks such as low noise amplifiers (LNA), mixers and voltage-controlled oscillators (VCO) are readily implemented in CMOS. However, RF power amplifiers (PAs) are a major roadblock in these efforts to create highly integrated system-on-chip, due to both the low breakdown voltage of the transistor and lossy substrate associated CMOS technology. Therefore, the PAs for high data rate wireless communication systems have been required high efficiency and linearity at the back-off power levels to efficiently amplify a multiplexing signal.

Thus, aware of the above problems, a cascode configuration and thick gate-oxide transistors have been used to eliminate the effects of oxide breakdown voltage and carrier degradation, allowing the use of a larger supply voltage. Moreover, the output-stage is composed of a main amplifier with class AB bias and an auxiliary amplifier with class C bias, which can improve linearity and reduce current consumption in the low power region. In particular, an integrated diode linearization technology provides the compensation mechanism for the input capacitance variation of the active devices to enhance the linearity of the CMOS PAs [1]. A second harmonic tank and optimum gate biasing point are applied for the cancellation of the nonlinear harmonic generated by [2].

Thus, this paper describes some improved PA design techniques to realize high power and high efficiency in a small area using the standard 40nm CMOS technology. In order to demonstrate the improved methods, a conventional PA and an improved one are compared for the P, PAE.

The paper is organized as follows. Section 2 describes the configuration and the operation principle of the proposed un-even biased HPA. The circuit design methodology will be discussed in Section 3, the simulation results are presented in section 4. Finally, section 5 provides a conclusion of this paper.

2. Design and Implementation

Fig. 1 shows the simplified block diagram of the proposed PA. It is a two-stage design of a programmable gain amplifier (PGA) for output power adjustment and a high power amplifier (HPA) for high linear operation. In addition, a balun is designed for impedance transforming and for combining the differential signals to a single load.

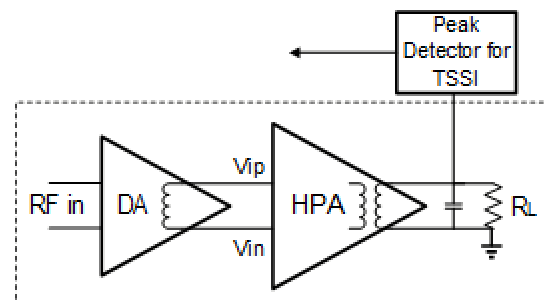


Figure 1. Simplified block diagram of the two-stage PA design

* Corresponding author: wangcheng1992@sjtu.edu.cn

The HPA stage and PGA stage employ a pseudo differential double cascode structure .The differential configuration is less sensitive to the ground inductance and has better stability compared with a single-ended version.The transformer is designed using the HFSS to provide the optimal differential load impedance from a 50 Ohm antenna at the 2.4GHz center frequency based on load-pull technology.

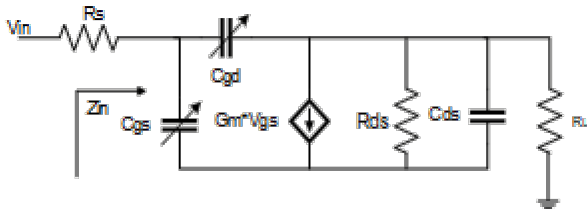


Figure.2. Nonlinearity model of NMOS power amplifier

As shown in Fig2.the two main sources of nonlinearity are Cgs and gm. The input impedance Zin is approximately as follows(1):

$$Z_{in} = \frac{1}{j\omega\alpha_{in}} = \frac{1}{j\omega[C_{gs} + (1+Av)C_{gd}]} \quad (1)$$

where Av is the voltage gain of the power amplifier. The relationship of Vgs and Vin is given by the following equation:

$$V_{gs} = \frac{Z_{in}}{Z_{in} + Z_s} V_{in} \quad (2)$$

As shown in equation(2), Vgs does not linearly increase with Vin and produce significant nonlinearity because Zin is not a constant parameter.

2.1 Operation Principle of Proposed un-even biased PA

Fig. 3 shows the principle of an un-even biased HPA. The input transistors of the output stage are separated into auxiliary and main transistor, and the gates of main and auxiliary transistors are biased at class AB and class C, respectively. The un-even biased method of combining two Gm stages (M1 and M2) with different gate bias is adopted for better linearization.M1and M2 transistors have different nonlinear characteristic and generate opposite polar third harmonics. According to [5],[6], the third harmonic nonlinearities are cancelled out by opposite phase combination, as shown in Figure.3. Moreover, when the input power is at the low power region, M2 does not consume the current . thus, the average efficiency can be improved in the overall power range.

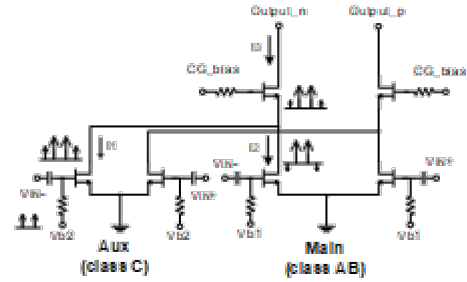


Figure.3 Simplified schematic of HPA and principle of gm3 cancellation

To obtain the optimized bias voltage ,the nonlinearity current(i_{ds}) can be expressed by the third-order Taylor expansion as follows:

$$i_{ds} = g_{m1} \cdot v_{gs} + \frac{g_{m2}}{2!} \cdot v_{gs}^2 + \frac{g_{m3}}{3!} \cdot v_{gs}^3 + \wedge \quad (3)$$

From the equation(3),the second harmonic and third-order inter-modulation can be expressed by the gm2 and gm3 as follows:

$$i_{ds,2\omega_2-\omega_1} = \frac{3}{4} g_{m3} v_{gs,\omega_2}^2 v_{gs,\omega_1}^* \quad (4)$$

According to [4], the third-order inter-modulation is generated from gm3. Thus, the strong nonlinear behavior can be reduced by setting the gate biasing of main and aux transistors close to A point and B point as indicated in Fig.4.

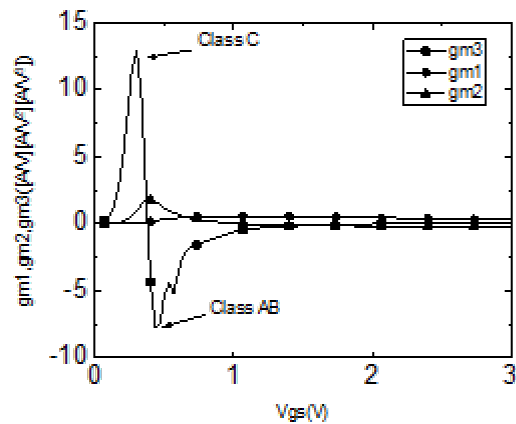


Figure.4. Calculated power expansion coefficients of gm at Vds=3.3V

However, due to the bias voltage of M2 is smaller than that of M1, the size of M1 and M2 should be optimized to obtain the proper linearization effect. though simulating drain current and power gain of the designed PA, respectively. In particularly, the proposed un-even biased technique can improve the average efficiency and linearity simultaneously by using M1 and M2 transistors with a 1:2 size ratio.

2.2The input-capacitance compensation technique for improving linearity

The integrated diode linearization technique is proposed. The advantages of this technique are small size and no extra dc current consumption.

To solve this problem, an integrated diode, linearization circuit is added between the bias and the gate of NMOS, as shown in Fig.5. Since the V_{in} gradually rises, the C_{gs} of input NMOS rises while the C_{gs} of the added transistor decreases. Thus the added transistor provides a cancellation mechanism for the distortion due to the nonlinearity of the input capacitance. As a result, the linearity of the HPA is improved

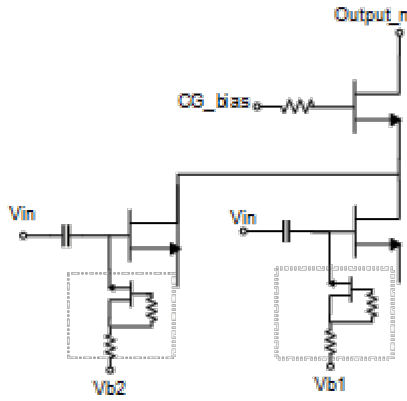


Figure.5. Simplified schematic of input-capacitance compensation technique

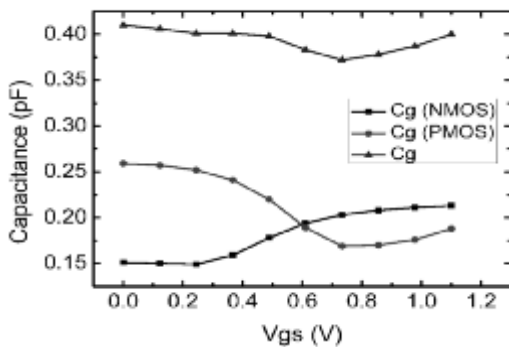


Figure.6. The capacitance of NMOS and PMOS

3. The simulation result

Fig.7 shows an overall schematic of the designed CMOS drive amplifier(DA) and high power amplifier (HPA).

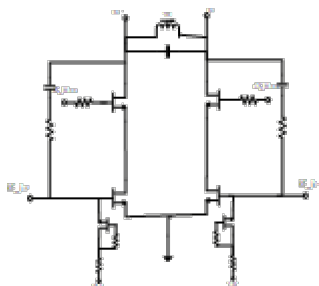


Figure.7. Schematic of the improved DA

This proposed circuit is simulated by the cadence software. To confirm the function of these improved techniques, a comparison of improved and conventional circuit in terms of 1 dB compressing point and PAE is

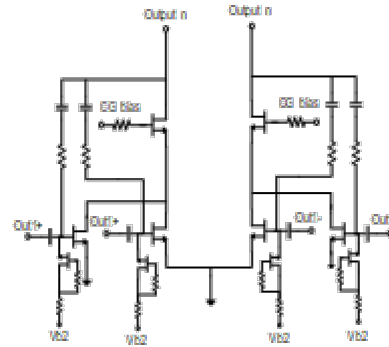


Figure.8. Schematic of the improved PA

shown in Fig 8 and Fig 9. The measurement was performed with a continuous wave single tone at a center frequency of 2.445 GHz. It reveals output P1db of 28.2dBm in the improved PA compared to the conventional PA, in which P1db of 27.1 dBm. This result shows the improved PA has 1.1dB higher linear range. As described in Figure 8, the PAE@P1db of improved PA and conventional PA is 32.4% and 26.1%, respectively.

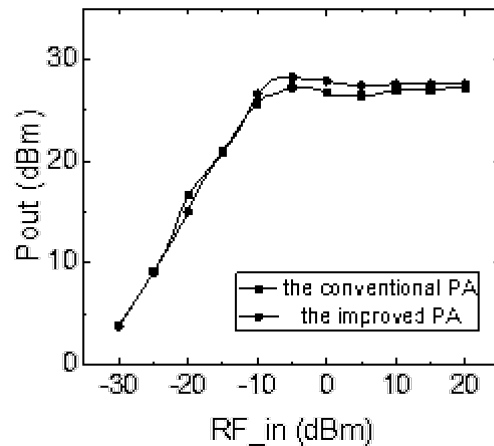


Figure.9. Comparison of Pout of the two types of PA

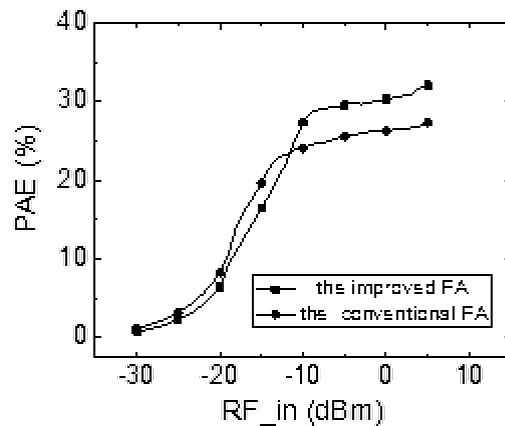


Figure.10. Comparison of PAE of the two types of PA. Finally, to compared the characteristic of the improved and conventional PA, the OFDM signal with a 20MHz channel bandwidth of 802.11g WLAN was applied. Fig.10 shows the measured ACPR at 25 dBm output power, the ACPR of the improved PA is 12.9dB better

than the conventional ,which confirms the two improved technique improving the PA linear characteristic. The performance of the improved PA is compared to the conventional PA in Table I. By using the proposed scheme in this work, the PA was achieved better performance.

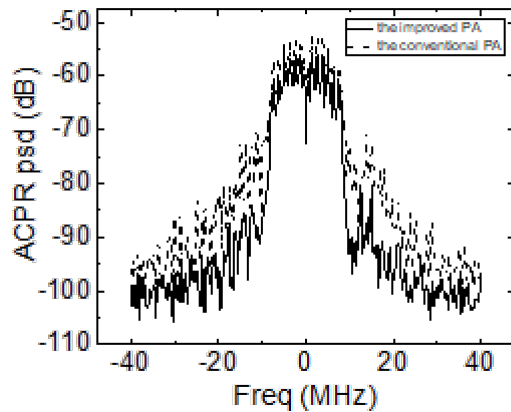


Figure.11. Comparison of ACPR of the two types of PA

Table 1. Comparison of PA

	Conventional PA	Improved PA
Supply voltage	3.3V	3.3V
(dBm)	27.1	28.2
PAE@P1dB	26.1%	32.4%
Power Gain@P1dB	37.5dB	36.4dB
Technology(CMOS)	40nm	40nm

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