Design and Simulation for a High-efficiency Class-B Power Amplifier

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Abstract. A class-B power amplifier with high output power and high power added efficiency (PAE) is designed in this paper. Based on the ADS tools of load-pull and source-pull, the optimal load impedance and source impedance can be obtained, respectively. Then, the matching circuit have been achieved by combining the impedance matching technique. Simulation results show that the class-B power amplifier has the PAE of 69.386% and output power of 45.32dBm with the working frequency of 960MHz. Therefore, It is a high-efficiency class-B power amplifier.

1 Introduction

Nowadays, all the major wireless standards-GSM, DMA,WCDMA, 802.11 a/b/g/n, WiBro and WiMax- are being integrated into a single package and widely adopted in the wireless communication system. A radio that integrates all of this functionality onto a single chip is urgently needed. One of the major impediments to addressing all these needs is the RF front end, specifically, the power amplifier (PA). That is to say, the compact and fully integrated radio frequency (RF) and microwave front-end products are the indeed demand for the rapid development of the wireless communication system. As a result, achieving simultaneously high efficiency and high linearity remains one of the major challenges in microwave PAs.

To our knowledge, PA is the core component of the wireless transmitter, its main function is to increase the RF power enough, which is effectively transmitted to a receiver through air medium. As the key equipment for the modern wireless communication, PAs have been widely applied in satellite communication, radar, wireless communications, navigation, electronic counter measures etc [1].

As mentioned above, in order to obtain the largest output power within a certain frequency range, the power transistor often works near the saturated state. At this point, its S parameters often change with the variation of the input signal, and the power gain will become smaller. In other words, the output/input of conjugate match gradually will become mismatching due to the small signal input. Then, it can not be able to obtain the maximum output power [2]. Therefore, the key point for PA design mainly lies in the design of matching network.

The technology of load-pull is the major method to find out the optimum load impedance corresponding to the largest output power. Meanwhile, the optimal source impedance can be obtained by the technology of source-pull. Finally, the output and the input matching circuit can be achieved, respectively.

Furthermore, comparing with the other PAs, Class-B PA has better linearity and higher power efficiency, for which its PAE can reach about 78.5% theoretically [3]. The DC working point for the power transistor of the class-B PA is often biased at the breakpoint [4], then the DC output current is zero. When the AC signal is used as the input, the power transistor switches on in a half cycle and switches off in the negative half cycle of AC signal. This operation mode of half cycle for class-B PA has remarkable advantages over Class-A PA. Moreover, the microwave field effect transistor (FET) of class-B PA can cause the increase of power efficiency and substantial reduction of both DC power and heat dissipation. Therefore, how to keep high efficiency and high power is the major challenge for the class-B PA.

The design strategies and implementation of a high efficiency class–B power amplifier based on the Freescale FET of MRFE6S9046 are presented in this paper. The simulation results show that the power additional efficiency (PAE) is 69.39% with output power of 45.32dBm when the input power is 26.5dBm in the working frequency of 960 MHZ. Thus, the demands of high performance and high efficiency can be achieved by comparing with the class-B PAs reported in exiting literatures.

This paper is organized as follows. The design of a high efficiency class-B PA is introduced in detail in Section II. Then its matching circuits of the source input impedances and the output impedances have been presented in Section III. In Section IV, the measured results of this PA are discussed as well as the conclusions.

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2 Design of the class-B power amplifier

The circuit schematic of the class-B PA based on the FET of Freescale MRFE6S9046 is given in Fig.1. It can be observed that it is consisted with the signal source, input matching circuit, power transistor, DC bias circuit, the output matching circuit and the load. Furthermore, based on the datasheet of this transistor, it can be known that when the PA works in the typical GSM mode. In this way, the DC bias circuit is used to set the appropriate working point for the power transistor. After simulation in ADS, The drain and gate of transistors were biased at 28V and 2.3V, respectively.

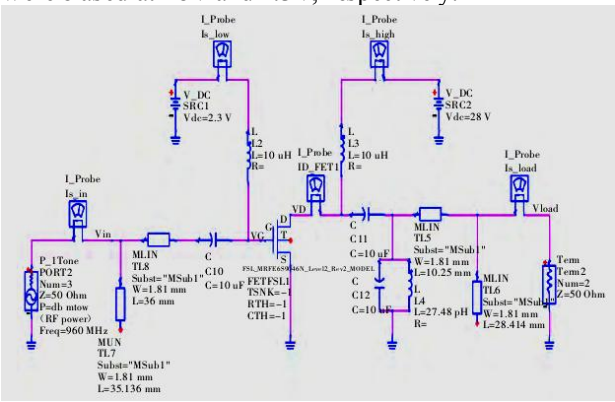

Fig.1 Circuit schematic of the class-B power amplifier

The PORT2 and Term2 in Fig.1 is the signal source and load, respectively. The DC bias circuit of the gate is consisted with SRC1, L2 and C10, where the voltage of SRC1 is the clip breakpoint voltage at the gate. L2 is used to switch on the DC signal and switch off the AC signal, and C10 is used to block the DC signal and conduct the AC signal. Similarly, the DC bias circuit of the drain is consisted with SRC2, L3 and C11. Where the voltage of SRC2 is 28V, L3 is used to conduct the DC signal and cut off the AC signal, and C11 is used to block the DC signal and conduct the AC signal.

Because the input matching circuit aims to match the optimal source impedance to 50 ohms, and the output matching circuit is used to match the 50 ohm to the optimal load impedance. In this way, TL5 and TL6 in Fig. 1 is used to match the optimal load impedance of 50 ohm based on the structure of micro-strip line, while TL7 and TL8 is used to achieve the matching for the optimal impedance to 50 ohm. The parallel resonance network which is consisted with L4 and C12 is used to determine the work frequency of the PA, which is 960 MHZ. And the parallel network is equivalent to open circuit at the working frequency, but it is equivalent to the short circuit for high order harmonic[5-6]. As a result, the PA has better function of filter.

After simulation in ADS, the optimal load impedance and source impedance corresponding to the maximum output power can be obtained using the load-pull and source-pull template. Here, the optimal load impedance and source impedance are 9.976-j*1.818 and 3.21-j*5.65, respectively.

3 Simulation optimization and analysis

To evaluate the S-parameters and validate the matching degree of the input and output matching circuit, this PA has been measured with small-signal and large-signal in ADS. Then the simulation curves of S11 and S21 at the room temperature of 25℃ for input match circuit and output match circuit can be obtained as shown in Fig.2 and Fig.3, respectively.

It can be seen that the PA achieves a gain approximately 18.2dB with S_{21} of less than −0.091dB and S_{11} of -39.55dB in the input matching circuit, as shown in Fig.2. Therefore, it can be concluded that the input matching network can realize the matching of optimal source impedance to 50 ohm.

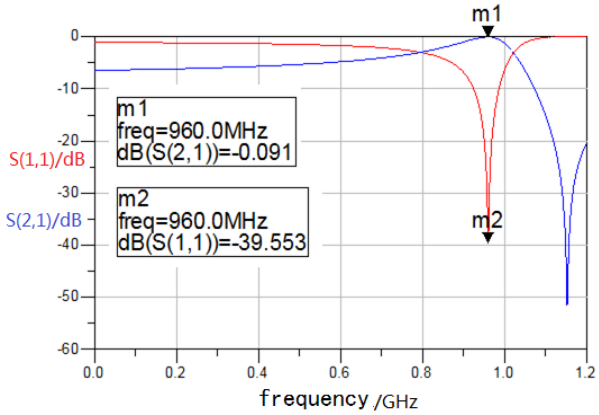

Fig.2 Performance of input match circuit.

Similarly, it can be found that the S21 is -0.026 and S11 is -38.86 at the frequency of 960 MHz in the output matching circuit from the Fig. 3. Therefore, the output matching network can realize the matching of 50 ohm to the optimal load impedance.

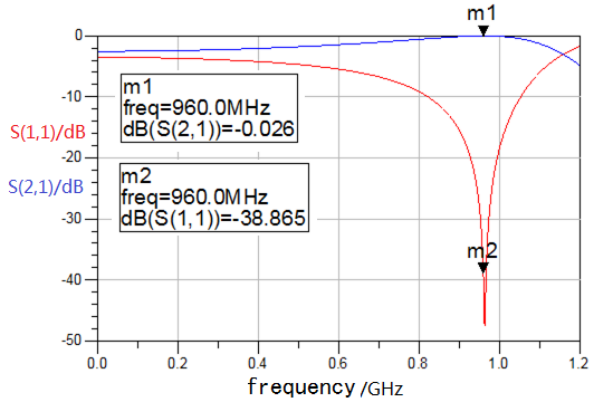

Fig.3 Performance of output match circuit.

Except for S parameter, PAE and output power are two important performance indexes for PA. Where PAE is used to measure the ability of converting the DC power into AC power for PA. The higher PAE means the better conversion efficiency [7]. Output power is the load power for the fundamental wave frequency signal. The higher output power, the greater power for the load and there is enough energy to emit the fundamental wave signal. Therefore, the large-signal RF power has been measured under different frequencies of driving continuous wave (CW) signal to evaluate the RF

performance of this PA. Thus, the relationship of PAE and output power against input power for this PA can be obtained as shown in Fig.4 and Fig.5, respectively. From the Fig.4, it can be seen that PAE increases rapidly with the rise of input power, and then reaches to the maximum, finally it decreases with the continuous rise of the input power. Especially, when the input power is 26.5dBm, PAE is 69.386%. This is rather good for class-B PA.

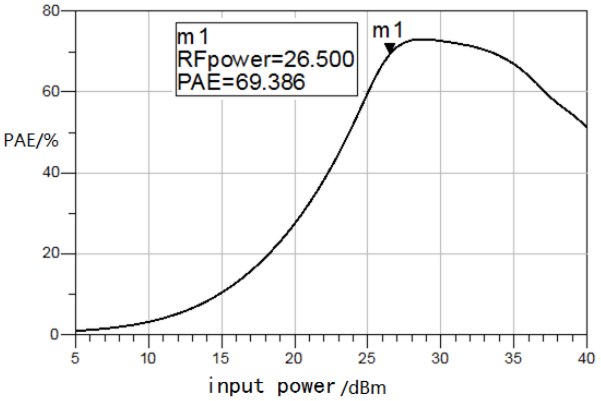

Fig.4 PAE against input power

At the same time, it can be observed from the Fig.5 that the output power increases linearly with the input power at the beginning. When input power reaches to 26.0dBm, the output power is almost invariant and keeps at the 47dBm. Especially, when input power is 26.5dBm, the output power is 45.32dBm. It is the most considerable index for class-B PA.

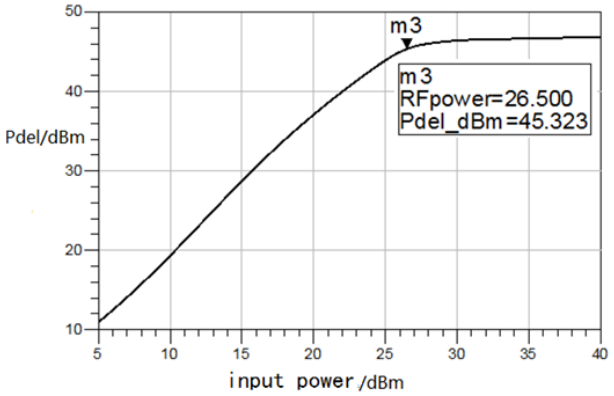

Fig.5 Output power against input power

Meanwhile, by scanning the input power, the waveform of U_{DS} and I_{DS} can be obtained as shown in Fig.6. The red sine curve clusters near the DC voltage of 28V are the waveforms of U_{DS}, While the blue curve clusters are the waveforms of I_{DS}, it is similar to the half sine wave in the vicinity of 0A. Moreover, because the transfer characteristic of the power transistor is not a straight line strictly, it is not the ideal half sine wave. At the same time, it can be seen that there is a interval of half cycle between the waveform of U_{DS} and I_{DS}. That is to say, when U_{DS} is big I_{DS} will become small and vice versa. In this way, the power of this FET would become smaller, then the DC power will be inverted into more useful load power. As a result, the power efficiency of this class-B PA can be significantly improved [8].

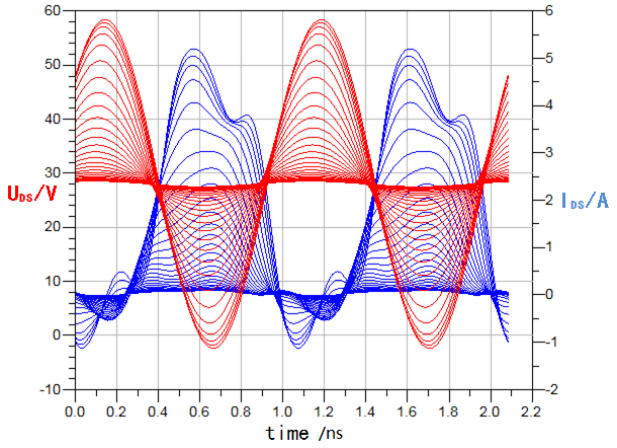

Fig.6 Waveforms of U_{DS} and I_{DS}

4 Results and discussions

In order to verify the truth that this class-B PA is high performance, the performace comparsion for all the designed class-B PA in the reported literatures has been summaried as shown in Table 1.

Table 1 Performance comparison of the class-B PA

References	Frequency (Hz)	PAE(%)	Output Power (dBm)	Gain (dB)
[9]	1G	45%	30.8	5.8
[11]	1.65G	40%	27.4	7.3
[10]	1.95G	27.4%	29.2	14.2
[12]	4G	44%	20	14.5
[13]	2.1G	72.8%	30.5	13.1
This paper	960M	69.39%	45.32	18.82

It can be observed that there are few research about the class-B PA and the operating frequency can reach several GHz with the increase of gain. The gain of this PA is the highest and the PAE is nearly 70%. It has achieved the high performance, but the frequency still needs to be improved.

5 Conclusions

A high-efficiency class-B PA based on the Freescale RF power FET of MRFE6S9046 is designed in this paper. After simulating and optimization in the ADS, it can work at 960 MHZ with output power of 45.32dBm and PAE of 69.386% when input power is 26.5dBm. Therefore, it can realize the high power efficiency and large output power and can be called the high-efficiency class-B PA.

Acknowledgements

This work is supported by Chun Hui Project of Education Ministry of China under the Grant Number of (Z2015033) and (Z2016071), the Apply Base Research Plan of Qinghai the Grant Numbers of (2017-ZJ-753), and the Undergraduate Teaching Research Project of Qinghai National University (2016-BKJXYB-09).

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