

Multi-channel monitoring approach of E1 streams

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Abstract. The object of development is a device for multi-channel monitoring of the E1 stream state. The subject of the development is the monitoring of the status of the channels and analysis of traffic in each time slot of the E1 stream. The purpose of this paper is to develop an approach that allows multi-channel monitoring of the E1 stream state.

1 Introduction

Transmission of telemetry data is an important task for a lot of companies. In most cases the data gathered by that equipment is extremely important, as proper systems' functioning and sometimes people's lives depend on its integrity. Thus, for the transmission of these data streams, it is advisable to use channel switches to which the E1 stream switches belong. The line data rate is 2048 kbps which is split into 32 timeslots, each being allocated 8 bits in turn, that makes the speed of each time slot 64 kbps. As a result, the total data speed rate in the E1 stream is 2048 Kbit / s. Out of 32 multiplexed channels two channels are used for frame synchronization and common channel signaling, where the service information necessary for the operation of telephone networks is transmitted. The remaining 30 channels are used to transmit digital information. Thus the application of E1 stream technology allows to organize 30 simultaneous independent communication channels in one physical stream. The relevance of the topic lies in the fact that solving the problem of monitoring the status of channels in the E1 stream and analyzing traffic in each time slot will allow to quickly detect violations in the equipment that generates incoming traffic E1 time slot analysis.

The modern digital primary network is built on the basis of three main technologies:

- Plesiochronous hierarchy (PDH);
- Synchronous hierarchy (SDH);
- Asynchronous transfer mode (ATM).

The PDH and SDH hierarchies interact through the multiplexing and demultiplexing of PDH streams into SDH systems.

The main difference between the SDH system and the PDH system is the transition to a new multiplexing principle. The PDH system uses the principle of plesiochronous multiplexing. According to which the procedure for equalizing the clock frequencies of incoming signals by the method of stuffing is performed for multiplexing, for example, four E1 (2048 kbit / s) streams into one E2 stream (8448 kbit / s). As a result,

when demultiplexing, it is necessary to perform a step-by-step process of restoring the original channels.

The E1 channel is the primary channel of the plesiochronous hierarchy. It is the main channel used in secondary telephony networks and data transmission. In comparison with the other channels of the PDH hierarchy, this channel has several features, namely the supercycle structure and the signaling channel. The remaining channels of the plesiochronous hierarchy have only a cyclic structure.

The structure of the E1 transmission systems includes three levels of the OSI model: physical, channel and network. The physical layer describes the electrical interface of the E1 stream, as well as the E1 signal parameters. The link layer describes the procedures for multiplexing and demultiplexing channels of a lower hierarchy level (bcc 64 kbit / s and PM channels) into the E1 stream, the cyclic and supercycloous structure of the E1 stream in the primary network, and monitoring error parameters at the network level. Let us consider in more detail the structure of each of the three levels of the E1 system. [1].

Basic scientific developments in monitoring errors in the E1 Data stream are presented by the authors: A. Vainshtein, YJ. Stein, F. Inumaru, N. Sato, K. Wakabayashi and etc. [2-5]

2 Proposed approach

As the review of existing methods and devices shows, there are several ways of monitoring the E1 flow. There are solutions that allow monitoring the status of the channels in the E1 stream, but the equipment analyzing the traffic in each time slot and allowing to display the contained information in these channel intervals is absent. For this reason, there is a need to create a device that will analyze the traffic in each channel interval, which will allow us to quickly detect violations in the equipment of the forming traffic for the analyzed E1 channel.

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Comparison of the methods used in cheap and expensive commutators for E1 stream analysis and the proposed method is shown in Table 1.

Table 1. Approaches overview.

Approach	E1 SYNC & MSYNC status	SNMP supported	The ability to track the status of time slots
Approach is used in cheap devices	yes	no	no
Approach is used in expensive devices	yes	yes	no
Proposed approach	yes	yes	yes

The device inputs to the transceiver block receive traffic from the E1 channels. Further, the obtained data is fed to the computing device for further analysis of the information contained in the received E1 channel. Thus, the error statistics in the E1 channels and the contents of their channel intervals are transmitted via the data bus to the SNMP server (Simple Network Management Protocol) [6].

The data received from the transceiver E1 is fed to the computing device further analysis is carried out of the information contained in the received E1 channel and a specific time interval. A survey of various materials has made it possible to distinguish three different ways of implementing a computing device:

- discrete digital elements of small and medium degree of integration;
- microcontroller or processor;
- digital microcircuit of a large degree of integration with a variable logic circuit.

Discrete digital elements of small and medium degree of integration include shift registers, coders,

decoders, encoders, decoders, multiplexers, counters, etc. All these elements are implemented in the form of separate chips, and if a small project may require a small number of chips, then for a large project the number of necessary chips becomes large, which also requires a lot of external connections. As a result, the complexity of the design, the dimensions of the printed circuit board increases, which is an essential drawback of this method.

Microcontrollers and processors allow processing of digital signals and implement complex algorithms, but the lack of microcontrollers is the sequential reception and processing of data. Since the task is to monitor eight E1 streams, data reception and processing should occur in parallel.

A digital IC of a large degree of integration with a variable logic circuit in this case has the advantage that the desired structure of the device is obtained by programming the connections of switching matrices, by controlling the bit sequence with logical keys. The control bit sequence is written to the internal static RAM during configuration, which gives the name to this class of programmable logic integrated circuits as FPGA (Field Programmable Gate Array). The peculiarity of this solution is that every time the power is turned on, the structure of the device is restored by recording in the internal static RAM. The advantage of using FPGA in this case is the ability to create adaptive systems whose structure dynamically changes with time, which allows the implementation of various digital devices on a single chip.

Summarizing the advantages and disadvantages of the considered ways of implementing the computing device, the optimal solution is to use the programmable logic integrated circuit of the FPGA type to develop an adaptive structure on a single chip [7]. As a communication bus the SPI [8] was chosen, as it has higher throughput than its competitors and extremely simple hardware interfacing.

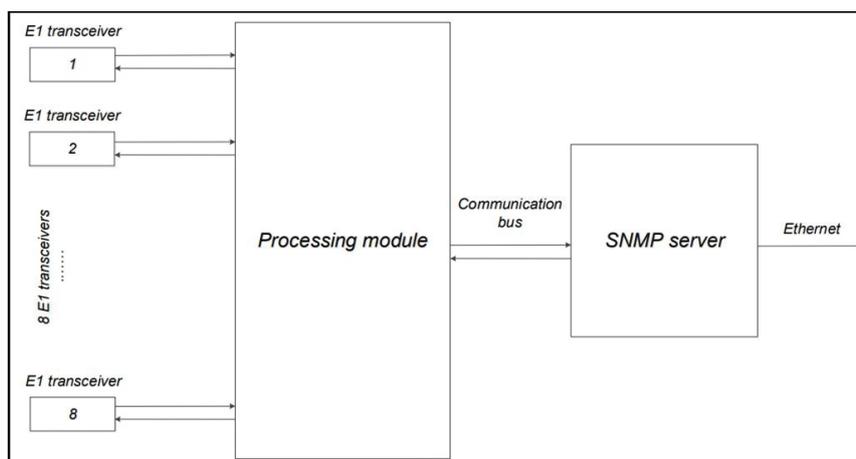


Fig. 1. Block diagram of the approach.

Based on SNMP server description, it has to have following capabilities:

- getting data from the communication bus;
- Ethernet transceiver, to send data to IP network;

- sufficient amount of RAM to store time slots errors and its content;
- fast processing unit for data processing.

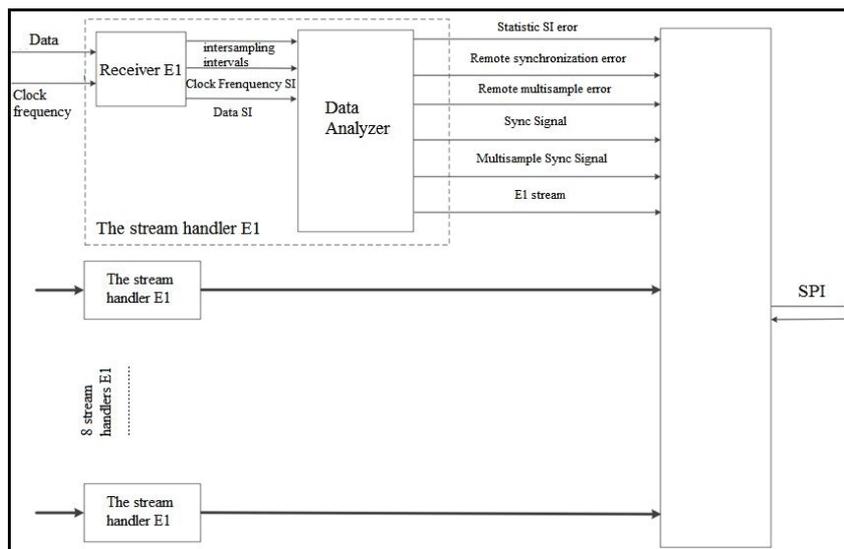


Fig.6. Block diagram of the time slot analyzer.

To test the functionality of the time slot [10] analysis unit, the built-in Quartus 2 modeling system was used[11]. The counter threshold is set as 5 data repetitions in one channel interval. Figure 7 shows that at the first repetition, the counter (count_repeats) increased by one, and became equal to 1.

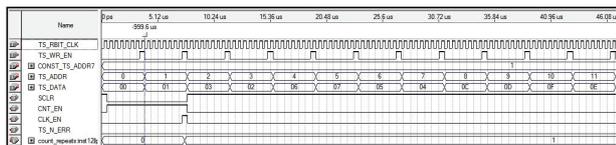


Fig. 7. Time diagram of the operation of the time slot analyzer.

In Figure 8 seen that at the next meeting of the repeating information in the first channel interval, the counter increased, and reached a threshold value of 5, which made the error signal (TS_N_ERROR) equal to one.

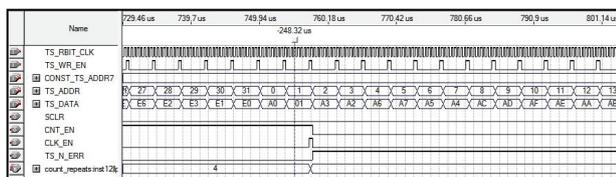


Fig.8. Time diagram of the operation of the time slot analyzer.

The modeling process provide the correct operation of the time slot analyzer.

4 Conclusion

As a result of this paper an overview of methods for detecting errors during the transmission of data through the E1 channel. The analysis of existing approaches used in devices that perform the monitoring functions of E1 stream and their shortcomings are revealed. A method was developed to monitor the state of the E1 stream based on the content in the time slots of the data stream.

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