Resistance requirements of threshold switching selectors in 1S1R crossbar array

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Abstract. Leakage current suppression ability of threshold switching selectors is important for the high-density crossbar array of resistive random access memory (RRAM). Nevertheless, incompatibility of selector with paired RRAM element will lead to serious problems during operation. This paper investigates the ON-/OFF- resistance requirements of threshold switching selectors with simulation in 1Mb array. Results show that OFF-resistance needs to be higher than certain value while ON-resistance needs to be lower than some value to make sure successful operation. In addition, it presents the method determining the appropriate resistance range in detail. It aims at proposing guideline for fabricating and choosing adequate threshold switching selectors before integrating with RRAM element economically.

1 Introduction

Resistive random access memory (RRAM) is one of the most promising candidates for next generation non-volatile memory. A two-terminal simple structure allows highly geometry scalability and fabrication in crossbar arrays. However, leakage current of crossbar RRAM array is one of the main obstacles for the high-density memory application. It can be effectively tackled by the addition of necessary nonlinearity to the RRAM by integrating a highly nonlinear and bidirectional selector device. This topology is known as the 1S1R architecture [1-3].

To date, selectors based on various mechanisms are proposed and mainly two kinds of I-V characteristics are observed for reported devices. Therein, Threshold switching selectors are widely concerned because of large nonlinearity and large drive current in the ON-state, including ovonic threshold switch (OTS) [4-6], metal-insulator transition switch (MIT) [7,8], field-assisted super-linear threshold switch (FAST) [9,10] and threshold vacuum switch (TVS) [11]. As figure 1, during forward voltage sweeps, it maintains high-resistive state (OFF-state) before threshold voltage (V_{th}) is achieved. When applied voltage surpasses threshold voltage, an abrupt and reversible transition occurs to conductive state (ON-state). During reverse sweeps, it transits to OFF-state after applied voltage is less than hold voltage (V_{hold}).

To investigate the impact of selector characteristics on the 1S1R crossbar array performance, IMEC compare various selectors and demonstrate that threshold voltage and ON-state resistance (R_{s_on}) are crucial parameters [12]. In addition, they studied the impact of resistance ratio of RRAM on the read performance of 1S1R array. They

took nonlinearity of tunneling selector into consideration [13]. Nevertheless the concrete resistance of selectors was neglected and they will lead to considerable effect to the array size and power consumption. As a result, it is essential to bring up the resistance requirements of selector before integrating the selector with RRAM. Meanwhile, it is economic and time-saving for fabricating an adequate threshold switching selector.

Figure 1 Schematic behavior of threshold switching selectors in voltage sweeps.

This paper is organized as follows. The simulation settings are presented in Section 2. The impact of ON- and OFF- resistance on array performance is analyzed in Section 3. In Section 4, appropriate ON- and OFF-resistance is determined. The conclusion is given in Section 5.

2 Simulation Setup

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2.1 Array configuration

The schematic of the simulated crossbar array is shown in figure 2 with fixed 1-Mb capacity (1024x1024). The word-lines (WL) perpendicularly intersect with bit-lines (BL) in a crossbar array with 1S1R cells built at the junctions. All RRAM elements and selector are identical without considering variability. Simulation is implemented using the worst case scenario for different read and write operation modes (Table I). The selected cell is located at the farthest distance from voltage source and ground. 1/2 bias schemes are adopted for single-bit read and write operation. Default line resistance is fixed at 5Ω/cell.

Table I Worst Case Data Pattern

Read HRS	Read LRS	Set	Reset
SEL: HRS	SEL: HRS	SEL: HRS	ALL LRS
WLHS: LRS	WLHS: LRS	WLHS: LRS	
BLHS: LRS	BLHS: HRS	BLHS: LRS	
NS: LRS	NS: LRS	NS: LRS	

Figure-of-merit (FOM) for read or write operation can be evaluated by read margin (RM), write margin (WM), read power (Pr) and write power (Pw). Read margin is defined as the ratio of readout disparity between HRS and LRS states over readout of LRS state. Write margin is defined as the ratio of voltage drop on selected RRAM over applied voltage. Read power and write power is the total power consumption of array in read and write process respectively.

Figure 2 Schematic of 2-D cross-point array. SEL: selected cell. WLHS: WL half-selected cell. BLHS: BL half-selected cell. NS: non-selected cell. $R_{wire}=5\Omega/cell$.^[12]

2.2 RRAM Model

The RRAM device is described using a parameterized template with fixed behaviour. As in figure 3, RRAM device can switch between a high-resistance (HRS) and a low-resistance state (LRS) by applying opposite voltage. For simplicity, both LRS and HRS are assumed being ohmic, where RHRS and RLRS are fixed at 500 kΩ and 50 kΩ respectively. It leads HRS/LRS resistance ratio equals to 10, which represents a typical resistance ratio for HfO_x-based RRAM device^[14]. The parameterized RRAM has symmetrical set and reset voltages of ±1.5V. Nonetheless, unintentional switching of practical devices occurs occasionally when applied voltage is less than write voltage. Disturb voltage is defined to determine the maximum voltage drop on the RRAM element, beyond

which the element state may change unintentionally. At this stage, default disturb voltage value is set to 1.0V.

Figure 3 Schematic I-V curve of RRAM element

2.3 Selector Model

Figure 1 represents a typical threshold switching selector behavior. Three parameters are employed to describe the threshold switching selectors, namely threshold voltage (V_{th}), OFF-resistance (R_{s_off}) and ON-resistance (R_{s_on}). For simplicity, in our model, OFF-state and ON-state are regarded as linear. The nonlinearity (NL) of selectors is defined as OFF-/ON- resistance ratio ranging from 1e3 to 1e5. In this case, once the selector is turned to ON-state, it will keep this state till the applied voltage is removed.

3 Analysis of Impact of ON- and OFF-resistance on array performance

Firstly, it is inevitable to generate adversary effect on array performance if resistance of selector cannot meet the requirements. When the array is prepared to operate, all the selectors are in OFF state. At this point, applied voltage will lead to large leakage current if OFF resistance is not high enough. While considering the line resistance, leakage current increases voltage drop on line, leading to the voltage/current loss. Then voltage on the farthest selected cell (as in table I) is not sufficient to turn on the selector, resulting in failed operation. When larger applied voltage is inflicted to solve the problem, voltage drop on unselected cell adjacent to the apply port may surpass the threshold voltage to switch on the selector, increasing leakage current and power consumption, even leading to false operation. Hence, it can be determined that in an array with certain size and threshold voltage of selectors, OFF-resistance of selectors cannot be less than some value lest for adversary effect on performance.

Secondly, during set/reset operations, although OFF-resistance is adequate to turn on the farthest selector, there may be other problems. For example, RRAM splits the voltage with selector in ON-state. If the ON-resistance is rather large leading to less voltage drop on RRAM, it still fails to switch the RRAM. In addition, during read operation, large ON-resistance will reduce the read margin, increasing difficulty of discriminating the HRS and LRS of RRAM. Then it can be determined that ON-resistance of selectors cannot be less than some value. In addition, most voltage will drop on RRAM after paired selector turned on. If threshold voltage of selector

is much larger than disturb voltage of RRAM, then voltage drop on RRAM may surpass the disturb voltage. In order to avoid above-mentioned situation, ON-resistance of selectors should be adequate to make sure the appropriate voltage division.

As a conclusion, OFF-resistance must be larger than certain value and ON-resistance must be less than some value to make sure smooth read/write operation. Meanwhile, in order to prevent false write during read, ON-resistance must be also larger than some value. Corresponding simulation process of 1/2 bias scheme is as follows: 1) fixing the threshold voltage, reset simulation determine the required minimum OFF-resistance and corresponding maximum ON-resistance; 2) based on the results of step 1), read simulation verify the read margin of the minimum OFF-resistance and corresponding maximum ON-resistance, determine the maximum ON-resistance; 3) read simulation determine the minimum ON-resistance to assure the voltage drop on RRAM less than disturb voltage with voltage division; 4) changing the threshold voltage and repeating above process.

4 Appropriate ON- and OFF- Resistance

4.1 Minimum OFF-resistance determination

In order to explore minimum OFF-resistance, simulation of reset process is implemented as follows: 1) fixing the threshold voltage, determining the maximum applied voltage less than double threshold voltage lest unselected selectors are switched on; 2) assuming the ON-resistance as 1 ohm, then all voltage will drop on the RRAM after paired selector is turned on, determining the minimum OFF-resistance and corresponding maximum ON-resistance by iterative calculation; 3) changing the OFF-resistance larger than minimum OFF-resistance, calculating corresponding maximum ON-resistance.

Figure 4 (a) Relationship between minimum OFF-resistance and threshold voltage; (b) relationship between reset performance and OFF-resistance

As can be seen from figure 4(a), minimum OFF-resistance decreases with the increasing threshold voltage. It can be deduced that with the increase of threshold voltage, bearable applied voltage increases. Then according to the analysis in section 3, larger applied voltage will reduce the requirement of minimum OFF-resistance. Although there is larger leakage current and voltage decay, larger applied can make sure enough voltage drop on the selected cell to operate. As a result, once the OFF-resistance is larger than the critical one, reset operation can be successfully implemented. In

addition, according to figure 4(b), if threshold voltage is fixed as 1.0V, relationship between array performance and OFF-resistance is analyzed. Larger OFF-resistance leads to lower leakage current and less power consumption. In addition, most of the voltage can drop on the selected cell, increasing write margin. This is in accordance with the instinct that larger OFF-resistance is better.

4.2 Maximum ON-resistance determination

Simulation of reset process can be utilized to evaluate the required maximum OFF-resistance, but also to deduce corresponding maximum ON-resistance because ON-resistance will affect the voltage division after selector turns on. As can be seen from the figure 5, under fixed threshold voltage, maximum ON-resistance increases with increasing OFF-resistance and level off finally. When maximum applied voltage corresponding to respective threshold voltage is applied, larger OFF-resistance will reduce leakage current and voltage decay. Then voltage drop on the selected cell increases and larger ON-resistance can also make sure that the voltage division on the RRAM is sufficient to switch. However, with further increase of OFF-resistance, leakage current cannot be reduced obviously. As a result, voltage drop on the selected cell cannot increase and maximum ON-resistance cannot increase as well. In addition, when threshold voltage decreases, applied voltage can be reduced then probability of false writing is lower during read operation.

Figure 5 Relationship between maximum ON-resistance and OFF-resistance and threshold voltage

5 Conclusion

ON-/OFF-resistance of threshold switching selectors severely affect array operation and performance. Controlling impacts of the appropriate resistance range is proved to be essential before integrating selector and RRAM element. In this work, we analyse the possible impact of ON-/OFF-resistance of selectors. Meanwhile, we propose a method to determine minimum and maximum ON-resistance and OFF-resistance in crossbar array. Results show that threshold switching selectors must satisfy the requirements of minimum OFF-resistance and maximum ON-resistance. This proposes

guideline for fabrication and option of appropriate selectors.

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