The Design of Nonlinear Chirp Based on the DSP Builder Technique

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Abstract. This paper, by analyzing the function Chirp, studies the software design and realization of the function. It offers a design plan based on the nonlinear Chirp signal of DSP Builder technique and designs the signal generator of the nonlinear Chirp based on the design flow of Matlab/Simulink/DSP Builder/QuartusII. It also conducts simulation verification using the development software Matlab/Simulink and QuartusII, proving that the design can well realize the signal source Chirp. The experiment proves that the DSP Builder technique can modify the starting frequency, bandwidth and the frequency resolution of linear frequency modulation signals by changing the programming parameters. The method is proved to be simple in designing, convenient in modification, low in cost and it doesn't involve any programming; therefore, it is easy to realize.

1 Introduction

The non-linear FM pulse signals are the ones whose instantaneous frequencies change with the time, i.e., the sine waves whose instantaneous frequencies change with the time in a range1.They are widely used in such fields as communication, radar, sonar for their wonderful bandwidth efficiency[2]3.The study of the realization of the wireless fuze signals Chirp in FPGA is significant for the research of wireless fuze system4. The test of stress waves based on the theory of chirp signals is widely used in engineer quality nondestructive testing. A large number of experiments have proved that the testing instruments developed on the basis of the study are effective in engineer testing.

Most of the Chirp signal sources commonly used in the current market are designed with the dedicated chips DDS[5]5[7]. They have wide output frequency and excellent high frequency performance. But they cannot meet the requirements for the fixed signal wave forms, functions and controlling modes produced by the dedicated DDS chips. Therefore, it is desirable to integrate one or several DDS core circuits and the other parts on a FPGA by using a programmable logic device. In this way, programming can be done on the chip and will be highly flexible and reconfigurable.

2 Math model analysis of Chirp signals

2.1 Chirp mathematical expression

The instantaneous frequencies of Chirp change with the time, i.e., it is a time function. Its math expression is as follows.

$$x(t) = \cos(2\pi \cdot f(t) \cdot t + \theta_0) \tag{1}$$

The Chirp functions can be divided into two types: linear chirp function and nonlinear chirp function according to the gradation rules of the Chirp output frequencies corresponding to the sampling time. The following two diagrams show the two chirp functions.

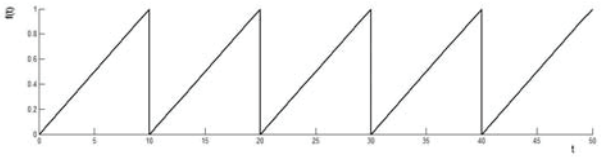

Fig1. linear chirp function

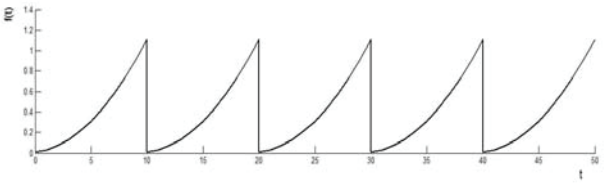

Fig2. Non-linear chirp function

From Fig.1 and Fig.2, we can generalize the closed system $f-t$ relation of Chirp function's frequency output and the time as follows:

For the linear Chirp function, the relationship expression in a continuous time domain can be:

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$$f_{out} = \kappa t + f_0 \quad (2)$$

In equation 2, κ is a constant, f_0 is the initial output frequency, t means the continuous time. The relationship expression in a discrete time domain is:

$$f_{out} = \kappa n + f_0 \quad (3)$$

In equation 3, κ is a constant, f_0 is the initial output frequency, n is a sampling site.

For the non-linear Chirp function, the relationship expression in a continuous time domain is:

$$f_{out} = f(t) + f_0 \quad (4)$$

In equation 4, $f(t)$ is nonlinear functions, f_0 is the initial output frequency; t is continuous time。In discrete time domain, there is relation formula:

$$f_{out} = f(n) + f_0 \quad (5)$$

In equation 5, $f(n)$ $f(t)$ is nonlinear functions, f_0 is the initial output frequency; n is a sampling site.

For nonlinear (Nonlinear) chirp functions, it is actually the quadratic function of the instantaneous frequency of signals, which can be expressed as a function:

$$f(t) = f_1 + f_2 t + (f_3 / 2)t^2 \quad (6)$$

In equation 6, f_1 is the static (fixed, initial etc) frequency, f_2 is the Doppler frequency, and f_3 is the conversion rate. When f_3 is 0, secondary FM signals are degraded into linear FM signals, so the sine and cosine signals and linear FM signals are the specials cases of secondary FM signals.

2.2 Phase-amplitude analysis

After the digitization of ADC, the expression of the quadratic frequency modulation signal is (sampling frequency f_0):

$$x[n] = \cos(2\pi(f_1 + \frac{f_2}{f_0}n + \frac{f_3}{2f_0}n^2)\frac{n}{f_0} + \theta_0) \quad (7)$$

By equation 7, it can be seen that the instantaneous phase:

$$\theta[n] = 2\pi(\frac{f_1}{f_0}n + \frac{f_2}{f_0^2}n^2 + \frac{f_3}{2f_0^3}n^3) + \theta_0 \quad (8)$$

In order to simplify equation 8, if

$$y_1[n] = \frac{f_1}{f_0}n + \frac{f_2}{f_0^2}n^2 + \frac{f_3}{2f_0^3}n^3$$

$$y_2[n] = y_1[n] - y_1[n-1] = \frac{2f_2}{f_0^2}n + \frac{3f_3}{2f_0^3}n^2 - \frac{3f_3}{2f_0^3}n + \frac{f_1}{f_0} - \frac{f_2}{f_0^2} + \frac{f_3}{2f_0^3}$$

$$y_3[n] = y_2[n] - y_2[n-1] = \frac{3f_3}{f_0^3}n + \frac{2f_2}{f_0^2} - \frac{3f_3}{f_0^3}$$

$$y_3[n] - y_3[n-1] = \frac{3f_3}{f_0^3}$$

Thus:

$$y_3[n] = c_3 + y_3[n-1] \quad (9)$$

$$y_2[n] = y_3[n] + y_2[n-1] \quad (10)$$

$$y_1[n] = y_2[n] + y_1[n-1] \quad (11)$$

Supposing $y_3[n]$ initial state is c_2, $y_2[n]$ initial state is c_1, $y_1[n]$ initial state is 0, thus $y_3[n] = c_3 n + c_2$

$$y_2[n] = \sum_{i=1}^{n}(c_3 i + c_2) + c_1 = c_3\frac{n(n+1)}{2} + c_2 n + c_1 \quad (12)$$

$$y_1[n] = \sum_{i=1}^{n} y_2[i] = \sum_{i=1}^{n}(c_3\frac{i(i+1)}{2} + c_2 i + c_1) \quad (13)$$

$$= \frac{c_3}{6}n^3 + (\frac{c_2}{2} + \frac{c_3}{2})n^2 + (\frac{c_3}{3} + \frac{c_2}{2} + c_1)n$$

Supposing:

$$Addr[n] = y_1[n] + c_0 \quad (14)$$

Thus:

$$Addr[n] = \frac{c_3}{6}n^3 + (\frac{c_2}{2} + \frac{c_3}{2})n^2 + (\frac{c_3}{3} + \frac{c_2}{2} + c_1)n + c_0 \quad (15)$$

The sine function values from $0 \sim 2\pi$ are divided into N parts, and the amplitude values on the points are stored in ROM. Then the phase values ωT are accumulated with a phase accumulator to figure out the current phase value and the current amplitude value is worked out by looking up ROM. The system chart is shown in Fig3.

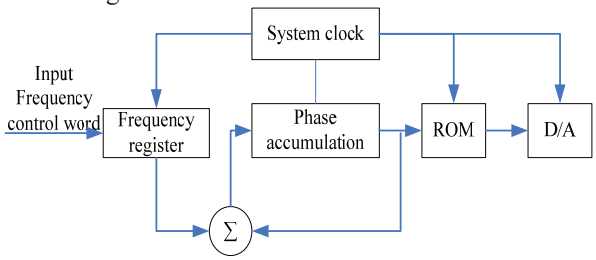

Fig3. System structure diagram of DDS

By searching ROM, the current amplitude can be worked out; then the output signals in table lookup by taking $Addr[n]$ as the address signal can be shown as follows:

$$x[n]=\cos(2\pi\frac{Addr[n]}{2^N})=\cos(2\pi \frac{\frac{c_3}{6}n^3+(\frac{c_2}{2}+\frac{c_3}{2})n^2+(\frac{c_3}{3}+\frac{c_2}{2}+c_1)n+c_0}{2^N}) \quad (16)$$

Compare with

$$x[n]=\cos(2\pi(f_1+\frac{f_2}{f_0}n+\frac{f_3}{2f_0^2}n^2)\frac{n}{f_0}+\theta_0)$$

,

$\theta_0=2\pi\frac{c_0}{2^N}$, $f_1=(c_1+\frac{c_2}{2}+\frac{c_3}{3})\frac{f_0}{2^N}$,

$f_2=(c_2+c_3)\frac{f_0^2}{2^{N+1}}$, $f_3=c_3\frac{f_0^3}{3\cdot 2^N}$ 。

The equivalent is:

$c_0=\theta_0\frac{2^N}{2\pi}$, c_0 is phase control word;

$c_1=f_1\frac{2^N}{f_0}-f_2\frac{2^N}{f_0^2}+0.5f_3\frac{2^N}{f_0^3}$, c_1 is frequency control word;

$c_2=2f_2\frac{2^N}{f_0^2}-3f_3\frac{2^N}{f_0^3}$, c_2 is Doppler frequency control word;

$c_3=3f_3\frac{2^N}{f_0^3}$, c_3 is Doppler change rate control word.

3 The algorithm realization

DSP Builder is a system-level (or algorithm level) design instrument provided by Altera. It is constructed on several software instruments and connects two design instruments: system level and RTL level. Therefore, it can bring the superiority of two instruments to their greatest play. It can help the designer fulfill the DSP design on the basis of FPGA6. Besides the graphic system modeling, DSP Builder can also achieve most design and simulation systematically, until the design document is downloaded on the DSP development board. According to equation 9, the model is set up using DSP Builder module under Matlab\Simulink89. The model is shown in the following figure 4.

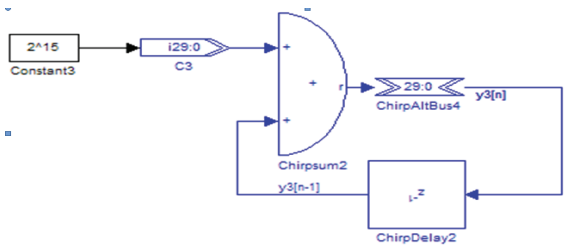

Fig4. Model of y3(n)

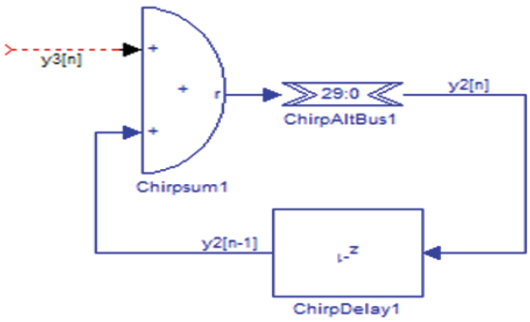

Fig5. Model of y2(n)

In Figure 4, the chirpsum2 is addition module, chirpDelay2 is Delay module, Implementation function of $y_3[n]=c_3+y_3[n-1]$. According to equation 10, Under Matlab\Simulink, the model is built with DSP Builder module, and the model is shown in the figure 5.

In Figure 5, chirpsum1 is addition module, chirpDelay1 is Delay module, Implementation function of $y_2[n]=y_3[n]+y_2[n-1]$.

According to equation 11, Under Matlab\Simulink, the model is built with DSP Builder module, and the model is shown in the figure 6:

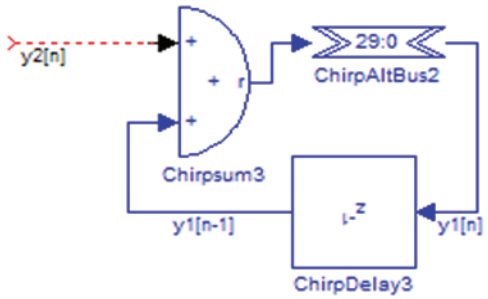

Fig6. Model of y1(n)

In Figure 6, chirpsum3 is a add-module and chirpDelay3 is a postponement module, which can realize the function in $y_1[n]=y_2[n]+y_1[n-1]$. According to equation 14, In order to realize the phase to amplitude conversion function, the model is built with DSP Builder module under matlab\simulink, and the model is shown in the Fig7.

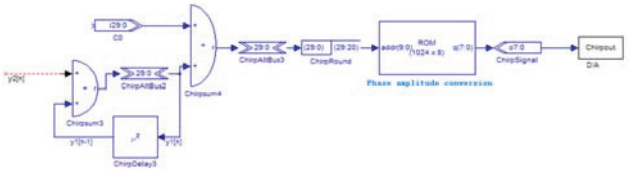

Fig7. Phase amplitude conversion circuit

4 Simulation analysis

After the simulation in Matlab/Simulink is ensured to be correct, the chirp signal model is transformed into VHDL language document using the Signal Compiler in DSP Builder so that it can be realized in FPGA. Figure 8 shows the result of the timing sequence simulation

conducted in QuartusII. Figure 9 shows the waves tested by embedded logic analyzer. It indicates that its waves are similar to the simulation waves of Matlab/Simulink and it confirms the correctness of the design.

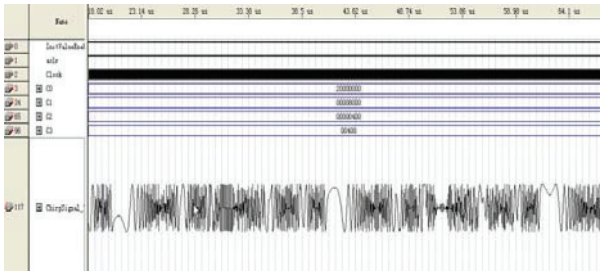

Figure 8 Timing simulation diagram in QuartusII

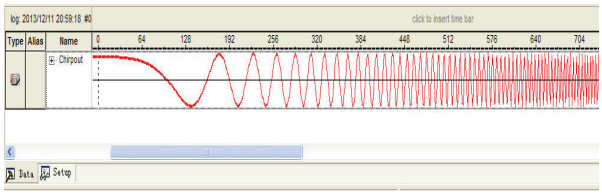

Figure 9 waveform measured by embedded logic analysis

5 Experimental Result

After the system is set up, the pin of FGPA is configured. Then it is translated and edited and the engineer document downloads the document •sof to the FPGA chips in the experiment box through the download cable. In this way, the Chirp signal generator is designed. The output side of the generator is tested with the Oscilloscope. Part of its waves are shown in figure 10.

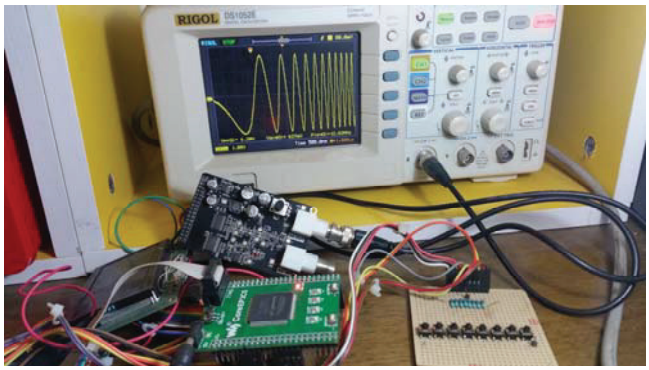

Figure 10 Chirp waveform observed by oscilloscope

From the figure 10 we can find that the frequencies of the Chirp signals designed in the way change obviously with the time, are considerably controllable and has good continuity in phases. Their functions and indicators are: 1) they can be used to generate sine waves with fixed frequencies and used in nonlinear FM; 2) the word length of the accumulator is 30, the output of the phase accumulator used to search ROM is 10 and the output word length of ROM is 8.

6 Conclusion

The paper studies the design plan of nonlinear FM pulse signals based on the technique DSP-Builder. It has simple system circuit, is extremely controllable and can be programmed repeatedly. Meanwhile, the design based on FPGA is highly readable and portable; therefore, it has good application prospect.

Acknowledgment

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