The Software Design of SiBCN Temperature Sensor Wireless Sweep Signal Receiving and Dispatching System Based on FPGA

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Abstract. SiBCN (silicon boron carbon nitrogen) wireless passive microwave resonant cavity temperature sensor is a new type of sensor under the development trend of radio frequency microwave technology. Based on the working principle of the sensor, the software design of SiBCN temperature sensor wireless sweep transceiver system based on FPGA is carried out on the basis of the existing wireless sweep signal transceiver system hardware. Let the signal source send the 11.0GHz ~ 11.6GHz range sweep signal to the sensor. The feedback signal of the sensor is filtered and the resonant frequency is obtained. The detection of temperature is based on the correspondence between the resonant frequency and the temperature. Through the analysis of the measured results, the system software design meets the requirements, and the temperature and frequency change rate is about 421.2KHz / °C.

1 Introduction

Temperature is a physical quantity prevalent in scientific experiments and industrial production, and temperature monitoring is required in many areas. However, in environments where the environment is extremely poor, such as in the aerospace industry, the temperature of the motor rotor and the aircraft turbine is extremely high and the conventional temperature sensing device can not detect it. Therefore, the design of a new type of high temperature temperature sensor detection system for many harsh environments temperature detection is of great significance. With the development of materials science, a temperature sensor based on SiBCN (silicon boron carbonitride) ceramic material was developed. The sensor is a new type of sensor under the development trend of radio frequency microwave technology, which has good high temperature thermal stability and anti-oxidation [1]. Figure 1 shows a top view and a side cross-sectional view of a SiBCN ceramic sensor.

Figure 1. SiBCN sensor overlooking and side view[1].

SiBCN temperature sensor resonant frequency will change according to the temperature shift, so the sensor works can be described as: The sensor in the full range of constant amplitude microwave scanning signal under the continuous excitation conditions, when the sensor contact temperature changes, the sensor dielectric constant will

follow the change, causing the cavity resonant frequency point offset[2]. Figure 2 shows the SiBCN sensor temperature principle demonstration.

Figure 2. SiBCN sensor test schematic.

2 Introduction to system software

The software design scheme uses the programmable logic device FPGA as the main control chip of the system. All peripherals of the control system, as well as the realization of digital signal filtering processing, all external device pins are connected to the FPGA and the FPGA unified allocation settings. FPGA software development using modular design, as shown in Figure 3 for the overall framework of the system software design. The software design mainly includes the following modules: HMC833 signal source module to control the transmission of the sweep signal; A/D module to complete the acquisition and processing of echo signals; SD card module to achieve data storage; host computer

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communication module, touch screen interactive module for the final system data waveform display.

Figure 3. Software module block diagram.

Figure4 shows the system software design process. After the system is started, the modules are initialized first. Then the control signal source generates the RF signal to sweep the sensor. The data of the sensor feedback is collected by the AD acquisition card and the median value filtering is carried out. When all the sweep ends After the series of mean values obtained by filtering, drawing the S11 curve, find the lowest point of the curve that is the minimum value of the feedback power to determine the corresponding resonant frequency point; and then the resonant frequency point into the corresponding temperature value, and through the touch screen to display.

Figure 4. System software design process

3 FPGA software design

According to the performance index and demand analysis of the sensor, the system software is mainly divided into two aspects: the sweep signal generating module and the echo signal acquisition and processing module.

3.1 Software Design of Sweep Signal Generation Module

The design of the signal source chip used by the Hittite company to produce a low phase noise, wide bandwidth fractional frequency-locked loop VCO chip HMC833. FPGA and HMC833 through the SPI interface protocol to communicate, to achieve the HMC833 internal register read and write control, control the signal source frequency of the launch, and by setting the relevant registers to achieve frequency automatic calibration function to ensure the accuracy of the transmission frequency [3].The output of the chip is:

$$f_{out} = \frac{f_{vco}}{k} \quad (1)$$

$$f_{vco} = \frac{f_{xtal}}{R} (N_{int} + N_{frac}) = f_{int} + f_{frac} \quad (2)$$

Type R: the reference branch frequency coefficient is set to 1 of the system; fxtal:the system reference frequency is set to 52MHz for phase;Nint:for integer frequency coefficient, Nfrac: fractional coefficient, software programming is achieved by changing the sweep frequency of integer frequency and fractional coefficient.

The software design of SPI communication is the prerequisite for controlling the signal source. Figure 5 shows the SPI bus write HMC833 internal register timing diagram. First, the master pulls high enable pin SEN while clearing SDI to enable SPI communication; then pull the SDI selection write operation when the first clock SCK comes; then send the next 30 clock falling edge 6-bit address bits and 24-bit data bits; finally pulled down. SEN to indicate that the write operation is complete.

Figure 5. SPI Write HMC833 Register Timing Diagram^[3]

After the completion of the SPI read and write communication function, the successful completion of the HMC833 chip internal VCO and PLL two sets of registers configuration, you can achieve the output of the RF signal. The REG 05H controls all the VCO register, for the output frequency setting signal source chip ratio and output power; while the PLL register is mainly used to control the signal source chip mode, which includes mode setting, fractional ratio coefficient setting[4]. As shown in Table 1, when the 5GHz signal is emitted by the signal source, the reference table of the register parameter value of the HMC833 in fractional frequency mode is given.

Table 1. HMC833 control register method table

Register number	Register value	Register number	Register value
REG 00h	0x0a7975	REG 0Bh	0x07c021
REG 01h	0x000002	REG 0Fh	0x000001
REG 02h	0x000001	REG 05h	0x000188
REG 03h	0x000060	REG 05h	0x00a090

REG 06h	0x200b4a	REG 05h	0x002898
REG 07h	0x00014d	REG 05h	0x0060a0
REG 08h	0xc1beff	REG 05h	0x001628
REG 09h	0x547fff	REG 05h	0x000000
REG 0Ah	0x002046	REG 04h	0x276276

As shown in Figure 6, the RTL view of the main program of the HMC33 signal source module. The float for the floating point processing module mainly realizes the register REG 03h and REG 04H (integer divider) (fractional) calculation, the hmc833_tx value of the hmc_833 internal register control module is used to configure the HMC833 chip register value, Spi_module is the communication module of SPI. It mainly realizes the function module of communication between FPGA and hmc833, and completes the writing of each register value.

Figure 6. HMC833 module total program RTL view

3.2 Software Design of Echo Signal Acquisition and Data Processing Module

The chip used for collecting echo signals is a precision AD9226 with 12 bits. The echo signal returned by the sensor is collected at the 1MHz sampling frequency, and the median filtering method is used to filter the collected data to obtain the valid mean value for each frequency. The final resonant frequency is determined by the three-stage sweep-frequency design.

Figure 7 for the AD9226 data acquisition timing diagram. The AD9226 uses a single clock signal to control the internal data conversion of the chip. It can be seen from the timing diagram that a sample value is acquired at the rising edge of each clock, and the sampling result is output after seven clock cycles. Programming control only need to provide the AD chip clock signal, no need for data communication to control it, and easy to use, the hardware only need to the 12-bit data pin and the clock foot and the FPGA corresponding to the pin connected, can achieve data acquisition [5].

Figure 7. AD9226 timing diagram [5]

In order to improve the validity of data acquisition, this design selects the median average filtering algorithm

for the digital filtering of ad data based on the actual situation of the system. The implementation process is first to sort the sampling sequences to generate sequences, and according to the actual data acquisition of the sequence of intermediate segment location value as the valid data region mean. The sorting algorithm is the key to achieve median mean filtering algorithm [6]. In view of the FPGA chip in the system has a sufficient amount of logic resources, the design uses a fully parallel sorting algorithm, using a large number of logic resources in exchange for the rate of sorting algorithm. Parallel four main steps are as follows: first of all the data synchronization algorithm are compared between each other, and according to the comparison result output 0 (small) or 1 (high); and then compare the results of steps to accumulate data on all data calculated for each sort of value; then the ranking values assigned to the corresponding sorting space; the final output results. In the 4 clock cycle, it can be completed all the data sorting process. As shown in Figure 8, the debugging results of the median value filtering algorithm based on full parallel sorting.

Figure 8. Data processing results

Three-stage sweep program specific process is to first sweep a large interval (3MHz), the number of 200 full-range sweep excitation. The starting frequency is 11.0GHz and the termination frequency is 11.6GHz. After the sweep, the data returned by the sensor is obtained by detecting the detector, and the corresponding frequency of the lowest point of the S11 curve is obtained by data processing, and the frequency is about 15MHz. A small interval (300KHz), the number of points of 100 for the second sweep, reducing the resonant frequency point of the search range; with the first paragraph of the sweep is similar to the detector by detecting the sensor to return the signal, and then determine a frequency, and here The frequency is about 5MHz for 3 times the small interval (100KHz), the number of points of the third paragraph of the sweep of the third paragraph of the three sweep is completed, the three sweep calculated by the S11 curve of the lowest point corresponding to the frequency value. The frequency value obtained by the mean value is the resonant frequency at the current temperature determined by the final temperature, and then the current temperature value is obtained by the correspondence between the sensor temperature and the frequency. Fig. 9 shows a graph of the three-step sweep S11, where (a) shows the first segment sweep S11, Fig. 2 (b) shows the second segment, and Fig. 3 (c) shows the third segment.

Figure 9. Three-stage sweep-frequency S11 graph

4 Analysis of system software performance and measured results

The performance of the system software is analyzed from the perspective of resource usage. As shown in Figure 10, an analysis of the use of resources after the system is compiled. A detailed description of the system using FPGA chip model and internal logic resources, pins, memory cells, embedded multiplier and clock management PLL consumption.

How Summary	
Flow Status	Successful - Tue Feb 28 15:07:41 2017
Quartus II 64-Bit Version	13.1.0 Build 162 10/23/2013 SJ Full Version
Revision Name	freq
Top-level Entity Name	freq
Family	Cyclone IV E
Device	EP4CE15F17C8
Timing Models	Final
Total logic elements	12,063 / 15,408 (78 %)
Total combinational functions	11,339 / 15,408 (74 %)
Dedicated logic registers	3,723 / 15,408 (24 %)
Total registers	3723
Total pins	33 / 166 (20 %)
Total virtual pins	0
Total memory bits	181,632 / 516,096 (35 %)
Embedded Multiplier 9-bit elements	4 / 112 (4 %)
Total PLLs	1 / 4 (25 %)

Figure 10. Analysis of the use of system resources

The temperature of the sensor is continuously changed from 25°C to a temperature of 350°C, and a temperature mark is selected at intervals of 25°C. Figure 11 shows the relationship between the resonant frequency and temperature. The results show that when the temperature increases, the resonance frequency decreases, and vice versa, the measurement curve is consistent with the characteristic curve of the sensor itself, which verifies the feasibility of the design.

Figure 11. The relationship between temperature and frequency

Conclusion

Based on the above software design, this paper designs a temperature detection system to achieve the temperature detection. Through the measurement, the system is in the temperature of 30~350°C, the frequency temperature change rate is about 421.2KHz/°C, the temperature update period 0.35s, in line with the expected requirements. But it still needs to be improved in accuracy. The system has good practical value and wide application prospect in the field of high temperature detection.

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