Novel Asymmetrical Pulse Width Modulation Method

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Abstract. The paper proposes new asymmetrical PWM that can be used for operation of multilevel inverters. The working and construction principle of this PWM is demonstrated on 13-level PWM signal that is applied to nine-level inverter and operates it as 13-level inverter. The proposed PWM signal consists of 5-level hybrid PWM which is constructed from two PWM signals- combined parts of the standard 5-level Phase Disposition (PD) PWM and pulsed PWM. The sum of these two PWM signals produces the desired 13-level PWM signal that is applied to the 9-level cascaded inverter. The proposed PWM method allows reduction of 13-level inverter components compared to the standard topologies such as neutral point clamped or flying capacitor inverters. This results in smaller size, weight and cists of the inverter.. Extensive simulation results validate the practicability of the proposed PWM method. The proposed method can be extended to any desired number of levels.

1 Introduction

The multi-level inverters have several important advantages upon 2- and 3-level inverters: they are suitable for high voltages and high power. The output voltage wave is built of several staircases that mitigate the voltage gradient dv/dt stresses on electric machine or transformer windings connected to the multi-level inverters. Furthermore, the output voltage wave has a much lower THD factor than that of the two-level inverters.

There are several basic configurations for multi-level inverters, and each of them has its advantages and disadvantages versus the others [1-4]. One of the configurations is the Neutral Point Clamped (NPC) multi-level inverter [5-8]. The distinct DC voltages are obtained by charging several capacitors from only one DC voltage source. The principal advantage is the need for only one DC voltage source. The principal disadvantage is the need to control and regulate the capacitor charging/discharging processes to ensure that their voltage levels remain quasi constant. Another distinct type of multi-level inverters is the Cascaded H-Bridge configuration [9-11]. In this topology, each inverter phase is built of several series connected H-bridges, while each H-bridge is supplied by its own DC voltage source. The principal advantage is stable voltage levels on the H-bridge active switches, which are fixed by the DC voltage sources, while their main disadvantage is the need for several DC voltage sources.

The paper presents the proposed multilevel asymmetrical PWM that is applied to 9-level cascaded NPC inverter and operates it as 13-level inverter. The proposed method is verified by extensive simulation results.

Section II presents the 9-level NPC cascaded inverter. Section III presents the proposed Asymmetrical PWM method. Section IV shows simulation results and their discussion. Section V presents conclusions of the paper.

2 The proposed inverter

The proposed 9-level inverter consists of two series cascaded 5-level and 3-level H-bridges on each inverter phase (see Fig. 1).

The first 5-level standard NPC H-bridge is fed by Vdc voltage source. The H-bridges uses a neutral point clamping approach to get 5-level phase voltages in place of the 3-level phase voltages commonly obtained with standard H-bridges. The 5-level NPC H-bridge inverter would be an optimal solution that compromises between the number of levels (5-levels), the number of separate DC sources and the cumbersome voltage control of the clamped neutral point [11–16]. The NPC control of the 5-level NPC H-bridges is performed by sensing the voltages on the clamping capacitors and the current direction. The suitable inverter state from its possible redundant states is chosen according to these measurements. By exchanging the capacitors, the switching algorithm balances the neutral point voltage. Without voltage balancing, one of the capacitors would charge to the full Vdc voltage and the other one would discharge to the zero voltage. The voltage levels of this H-bridge are 0, Vdc/2, -Vdc/2, Vdc and –Vdc. The second bridge is standard 3-level H-bridge fed by Vdc

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voltage source. The voltage levels of this H-bridge are 0, Vdc and –Vdc. If this inverter is operated by standard PD PWM, it provides nine voltage levels. The switching of the inverter in this case is shown Table I.

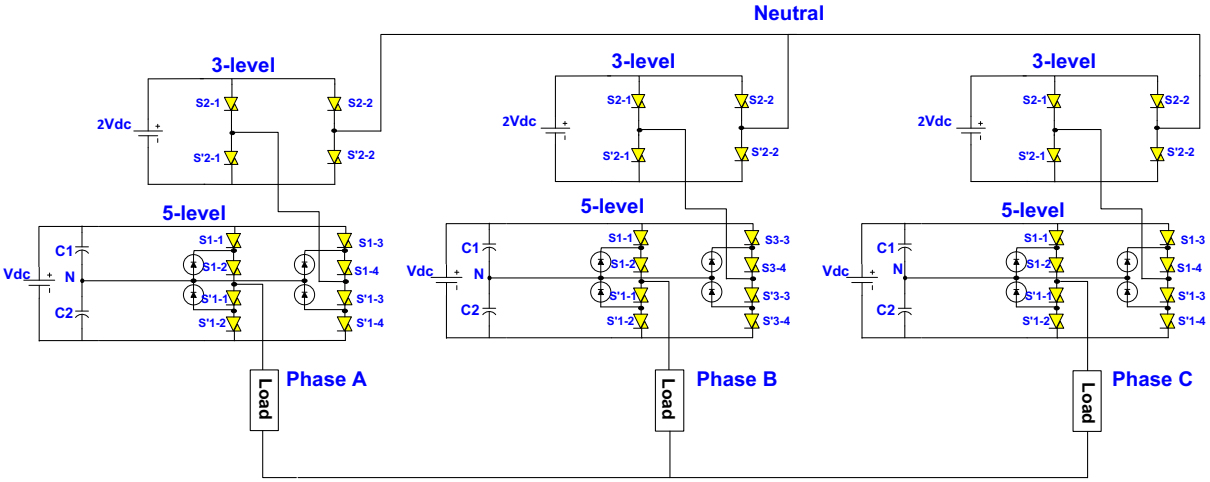


Fig. 1. The cascaded 9-level inverter.

Table 1. The switching states of the cacscaded NPC 9-level inverter when operated by PD PWM.

State	Switch/ voltage	S1-1	S1-2	S1-3	S1-4	S'1-1	S'1-2	S'1-3	S'1-4	S2-1	S2-2	S'2-1	S'2-2
1	0	0	1	0	1	1	0	1	0	1	1	0	0
2	Vdc/2	1	1	0	1	0	0	1	0	1	1	0	0
3	Vdc/2	0	1	0	0	1	0	1	1	1	1	0	0
4	-Vdc/2	0	1	1	1	1	0	0	0	1	1	0	0
5	-Vdc/2	0	0	0	1	1	1	1	0	1	1	0	0
6	Vdc	1	1	0	0	0	0	1	1	1	1	0	0
7	-Vdc	0	0	1	1	1	1	0	0	1	1	0	0
8	2.5Vdc	1	1	0	1	0	0	1	0	1	0	1	0
9	2.5Vdc	0	1	0	0	1	0	1	1	1	0	1	0
10	-2.5Vdc	0	1	1	1	1	0	0	0	0	1	0	1
11	-2.5Vdc	0	0	0	1	1	1	1	0	0	1	0	1
12	3Vdc	1	1	0	0	0	0	1	1	1	0	1	0
13	-3Vdc	0	0	1	1	1	1	0	0	0	1	0	1

3 The proposed Asymmetrical PWM method

This inverter can be operated also at 13-level voltage by application of the proposed asymmetrical PWM.

The proposed asymmetrical PWM method partially uses standard PD PWM method. In the standard PD PWM the comparison is performed separately for each phase of the inverter. The intersection points between the modulation wave and the carrier waves define the duty cycle or the switching instants of the inverter. This approach works excellently when the carrier frequency is much higher than the modulation frequency, e.g., about fifty to one hundred times higher. However, such higher switching frequencies would also yield rather high switching losses. Therefore, continuous efforts are made to lower the carrier frequencies together with raising the number of levels in multi-level inverters. The multi-level inverter of n levels uses n−1 carriers. For example, twelve carrier waves would be used with the present 13-level inverter and they are placed one upon the other. Generally, the carrier frequency is calculated according to:

$$f_{carrier} = 3(2k + 1) \times f_{modulation} \quad (1)$$

where k is a positive integer.

It is recommended that the frequency index be an odd number. Furthermore, the beginning phase between the carrier and the modulation waves should be the same for all the three phases of the inverter. Therefore, the frequency index should be a multiple of three. The proposed asymmetrical 13-level PWM signal is obtained by summing two PWM signals: the 5-level hybrid PWM signal and 3-level pulsed PWM signal. The first 5-level hybrid PWM signal is constructed from combined parts of the standard 5-level PD PWM (see Fig. 2) according to the desired pattern as shown in Fig. 3 (PWM signal for 5-level bridge). The second 3-level pulsed PWM signal is constructed in coordination with the first 5-level hybrid PWM signal is such a manner that the sum of these two PWM signals will be the desired 13-level

PWM (see Fig. 3, PWM signal for 3-level bridge). The desired 13-level PWM signal that is applied to the 9-level inverter is shown in Fig. 4.

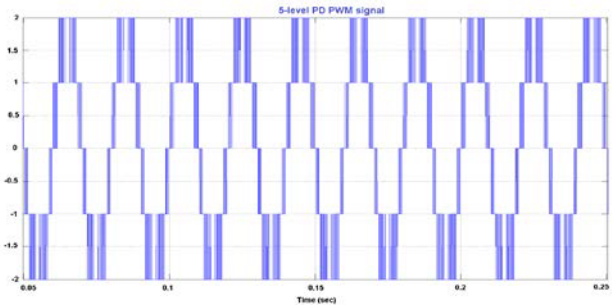


Fig. 2. The standard 5-level PD PWM signal.

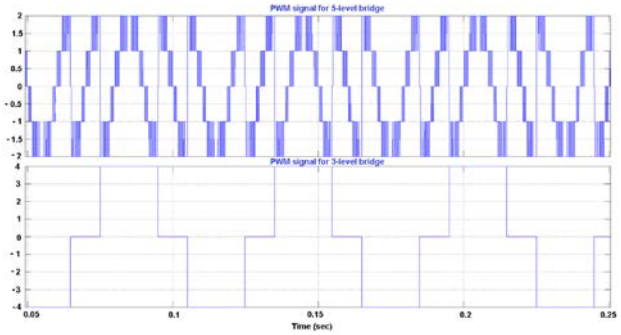


Fig. 3. The standard 5-level PD PWM signal.

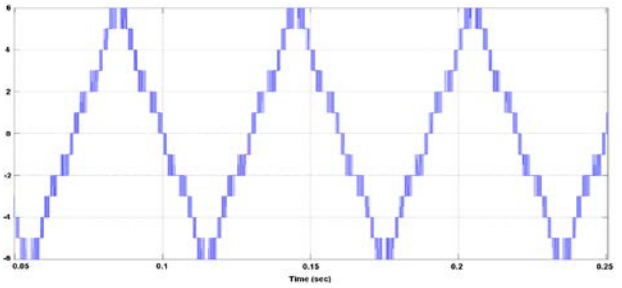


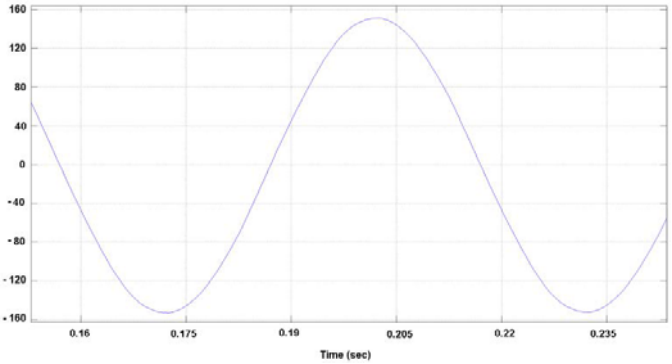
Fig. 4. The obtained 13-level PWM signal.

4 The Simulation results

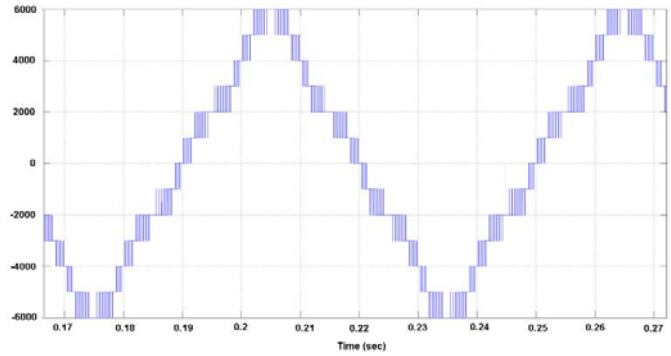
In order to verify the proposed PWM method, extensive simulations are performed. The simulation parameters are: DC=2000V, DC link capacitors C1=C2=10mF; the load of the inverter per phase are $R = 0.19\ \Omega$, L=0.24H.

During the simulation of this 13-level PWM signal, the modulation frequency was set to 50Hz and the carrier frequency to 2100Hz. The obtained 13-level PWM signal is applied to the presented 9-level inverter. If standard 13-level PD PWM was used, it would require additional cascaded bridge. This would result in additional costs and larger size and weight.

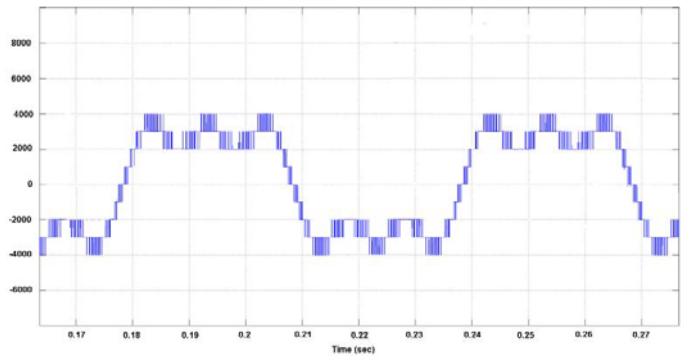
The proposed PWM was also simulated for different modulation indexes. The simulation results are shown in Tables II and III.



(a) Phase current, THD=0.9%



(b) Phase voltage, THD=16%



(c) Line voltage, THD=35%.

Table II. Output voltage and current THD versus the level number. Modulation frequency 50Hz, carrier frequency 1050 Hz, PD PWM

Modulation index	Inverter levels (modulation index)	Phase current THD (%)	Phase voltage THD (%)	Line voltage THD (%)
1	13-level (1)	0.9	16	35
0.83	11-level (1)	0.8	21	38
0.67	9-level (1)	1	27	44
0.5	7-level (1)	0.95	33	52
0.333	5-level (1)	0.8	47	61
0.167	3-level (1)	0.85	65	78

Table II shows that the decrease in the modulation index influences the number of the voltage levels in the output voltages, e.g., there are thirteen voltage levels in the phase voltage with modulation index 1, but only three voltage levels with modulation index 0.1. As a

result, the appearance of the output current and voltage waves changes as well as their spectra and harmonic content and distribution. Regarding the output voltage waves, it is seen that their waves better resemble a sinusoidal wave as the number of levels increases. As a result, their THDs decrease as well.

It can be seen that the proposed PWM method provides good THD results of the currents and voltages. The phase current THDs are below 1% which is in full accordance with IEEE 519 standard. Therefore, the proposed method is practicable and it can be implemented also to other multilevel inverter topologies. This PWM method can be extended to higher number of levels.

5 Conclusions

The paper proposes new asymmetrical PWM that can be applied to different types of multilevel inverters. The proposed 13-level PWM is constructed form the sum of two PWM signals. This PWM method operates 9-level inverter as 13-level inverter. As a result it allows reduction of the operated inverter's components compared to the standard topologies such as neutral point clamped or flying capacitor inverters. This results in smaller size, weight and cists of the inverter. However, the PWM control becomes more complicated compared to the standard PWM methods such as Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD).

It can be seen that the proposed PWM method provides good THD results of the currents and voltages. The phase current THDs are below 1% which is in full accordance with IEEE 519 standard.

Extensive simulation results validate the practicability of the proposed PWM method. The proposed method can be applied to any desired number of levels.

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