

# Warpage behavior analysis in package processes of embedded copper substrates

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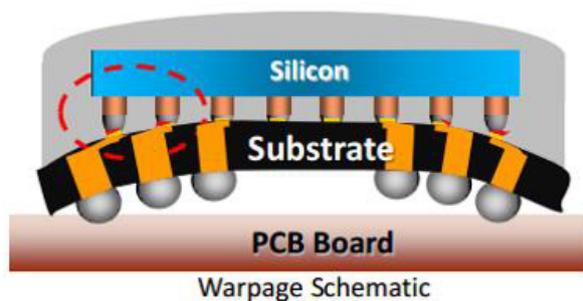
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**Abstract.** With the advance of the semiconductor industry and in response to the demands of ultra-thin products, packaging technology has been continuously developed. Thermal bonding process of copper pillar flip chip packages is a new bonding process in packaging technology, especially for substrates with embedded copper trace. During the packaging process, the substrate usually warps because of the heating process. In this paper, a finite element software ANSYS is used to model the embedded copper trace substrate and simulate the thermal and deformation behaviors of the substrate during the heating package process. A fixed geometric configuration equivalent to the real structure is duplicated to make the simulation of the warpage behavior of the substrate feasible. An empirical formula for predicting the warpage displacements is also established.

## 1 Introduction

Thermal bonding of copper pillar flip chip packages is a relatively new bonding process in packaging technology field, especially for a substrate with an embedded copper trace. During the heating package process of an embedded copper trace, the substrate warps at high temperatures as shown in Fig.1 [1]. These warpage causes a gap between the substrate and die, which will lead to welding failure.



**Fig. 1.** Warpage schematic during heating package process of an embedded copper trace.

Kim et al. [2] used an anisotropic shell model, considering their viscoelastic properties, to simulate the warpage behavior of a high-density multilayer printed circuit board for solid-state disk drive, with homogenized copper patterns. Both the maximum warpage and the residual warpage of the full microelectronic package were predicted.

McCaslin et al. [3] developed a methodology to predict the warpage of a particular substrate. The

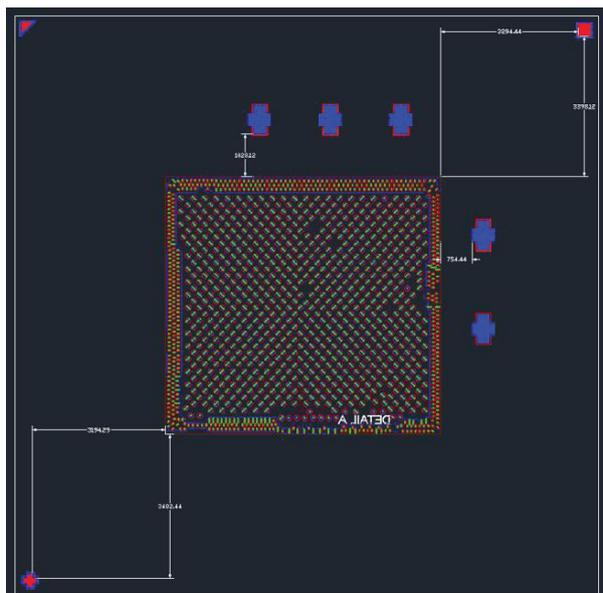
methodology accounted for both the trace pattern planar density and planar orientation in material property calculations for each layer of a multilayer substrate. Their results using the developed methodology agreed with the experimental data.

Tsai et al. [4] used shadow moiré method to measure the warpage of flip-chip PBGA packages subject to thermal loading. They used the finite element method and Suhir's theory [5] to analyze the thermal deformations of the package and discuss the mechanism.

The substrate geometry discussed in the literature was relatively simple, this study uses a Finite Element Analysis software ANSYS to simulate the embedded copper trace substrate and a model for analysis of thermal behavior at high temperatures is established [6]. An empirical reference formula from the finite element analysis results is established to predict product's warpage performances with its structure parameters.

In order to achieve this goal, there are two approaches; one is to simulate all substrate with its actual structure. The advantage of this method is the simulation results can reflect the warpage of the whole substrate. However, the actual structure of the substrate is very complicated and asymmetric as shown in Fig. 2, and it needs a lot of resources and spent a lot of time to finish one simulation. So another approach of simplifying the actual structure is used it to replace the complicated structure of the substrate. The entire structure is assumed to be homogeneous. The most important thing is that only a small part at the center of substrate is simulated, and then curve fitting is used to predict entire substrate's warpage performances [7].

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**Fig. 2.** Top view of substrate (red frame is the center of substrate).

## 2 Finite element modelling

### 2.1 Material properties

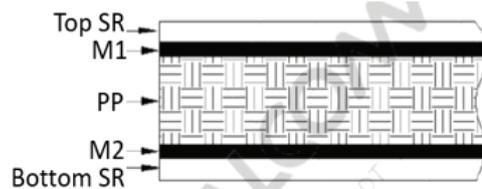
This substrate is composed of three kinds of materials: copper (Cu), polypropylene (PP) and solder resist (SR). The material properties are shown in Table 1. The coefficients are assumed to change linearly between the two temperatures.

**Table 1.** Material properties used in finite element simulations.

Material	Young's modulus (GPa)	CTE(ppm/°C)	Poisson's ratio
Cu	$E_c=110$	$\alpha_c=16.5$	0.34
PP	$E_{pp}=18(T=25^\circ\text{C})$ $E_{pp}=11(T=250^\circ\text{C})$	$\alpha_{ppx}=\alpha_{ppy}=12$ $\alpha_{ppz}=27$	0.18
SR	$E_{sr}=6.1(T=25^\circ\text{C})$ $E_{sr}=0.19(T=250^\circ\text{C})$	$\alpha_{sr}=45(T=25^\circ\text{C})$ $\alpha_{sr}=130(T=250^\circ\text{C})$	0.37

### 2.2 Geometric structure of substrate

The substrate structure can be roughly divided into five layers: top SR, M1, PP, M2 and bottom SR, as shown in Fig. 3.

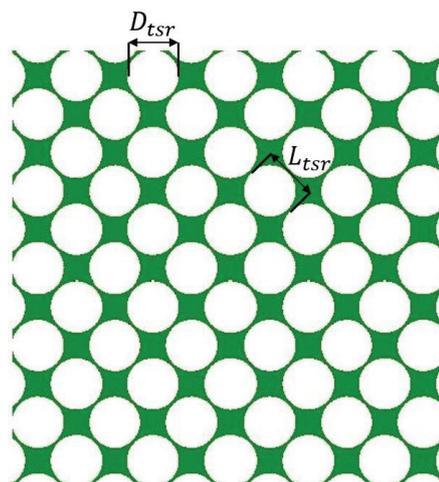


**Fig. 3.** Cross section schematic diagram of substrate.

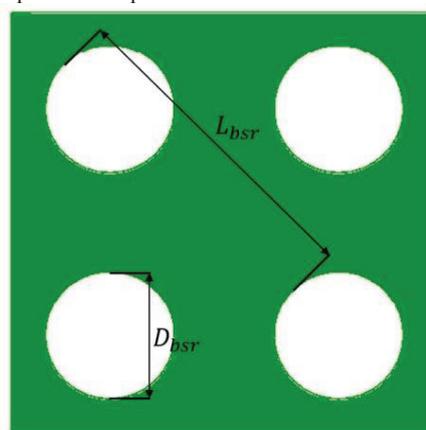
Top SR and bottom SR are solder resist, M1 and M2 are copper, and PP is Polypropylene. The configurations of each part are shown in Figs. 4-8.

The top SR and bottom SR have the same structures as real structure, but M1 and M2 are based on the copper area occupation ratio. Assume a square pad has a pitch of  $L_{M1}=L_{M2}=100\mu\text{m}$ , according to pitch and copper area occupation ratio,  $W_{M1}$  and  $W_{M2}$  for M1 and M2 can be determined.

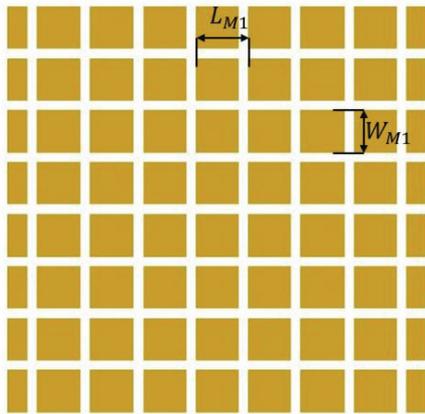
As the title, this is an embedded copper substrate, therefore, copper should be embedded into PP, so clearly there are many notches corresponds to M1 and M2 as shown in Fig. 8.



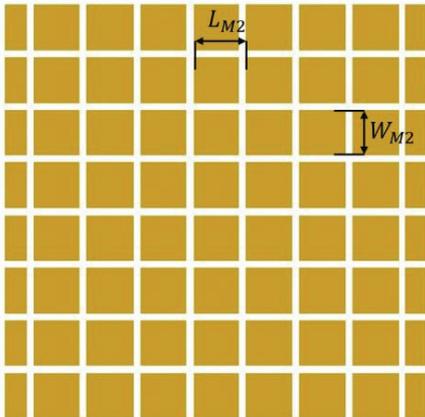
**Fig. 4.** Top view of top SR.



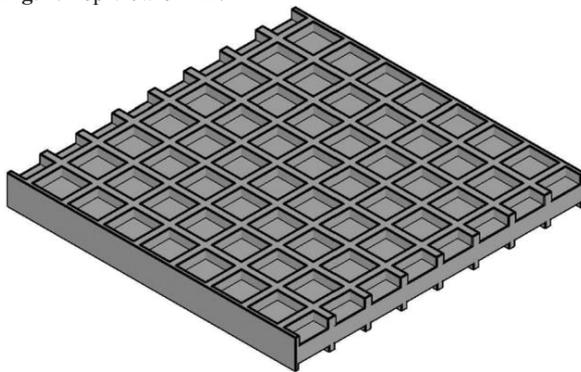
**Fig. 5.** Top view of bottom SR.



**Fig. 6.** Top view of M1.



**Fig. 7.** Top view of M2.



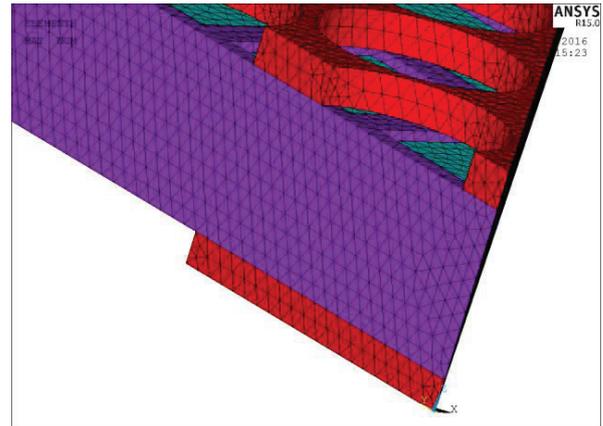
**Fig. 8.** Stereogram of PP.

### 2.3 Mesh setting and boundary condition

#### 2.3.1 Mesh setting

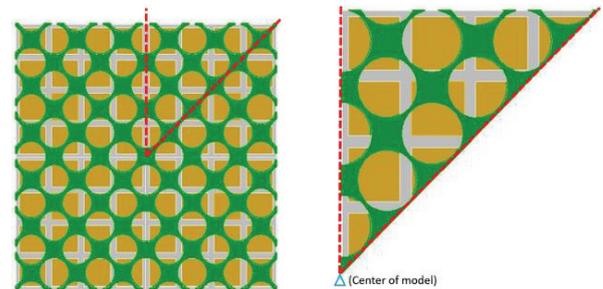
The model is auto meshed by tetrahedron 10 node element, and set the longest element edge length as  $7(\mu\text{m})$ . The mesh configuration is shown in Fig. 9.

Because this model is selected from the center of substrate, it has one-eight symmetry structure as shown in Fig. 10. In order to save resource and time, a symmetry boundary condition on the symmetry surface is set, and the node on the bottom of the substrate center is fixed, Gravity in all elements is not considered.



**Fig. 9.** Mesh configuration.

#### 2.3.2 Boundary conditions

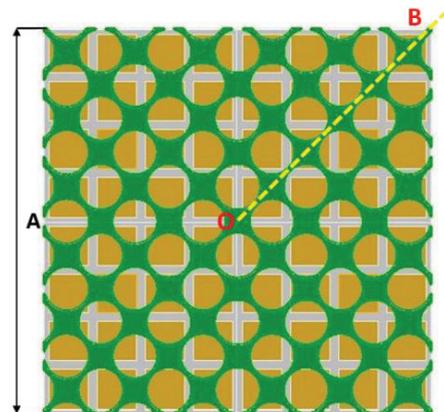


**Fig. 10.** Boundary condition.

The last boundary condition is temperature. In order to analyse substrate's warpage behavior during package process, the initial temperature is assumed at room temperature ( $25^\circ\text{C}$ ). The temperature are given as following: 50,100,150,183,217,245,260 $^\circ\text{C}$ .

### 3 Results and discussion

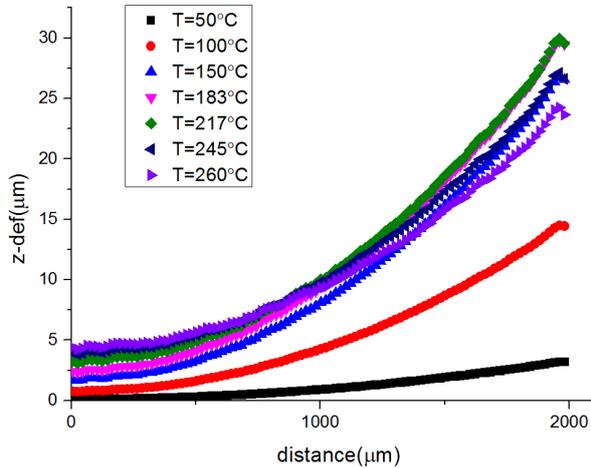
The displacements at the thickness direction on the diagonal line are measured as shown in Fig. 11. Using these results, curve fitting and expansion to entire substrate scale are established.



**Fig. 11.** Select displacement of thickness direction on diagonal line OB.

The displacement distributions on the diagonal line OB (shown in Fig. 11.) for all temperatures are shown in Fig. 12., diagonal line OB is set started from O end to B (distance 0 to 2000). Based on these displacement values, quadratic equations are used for curve fitting as shown in Table 2.

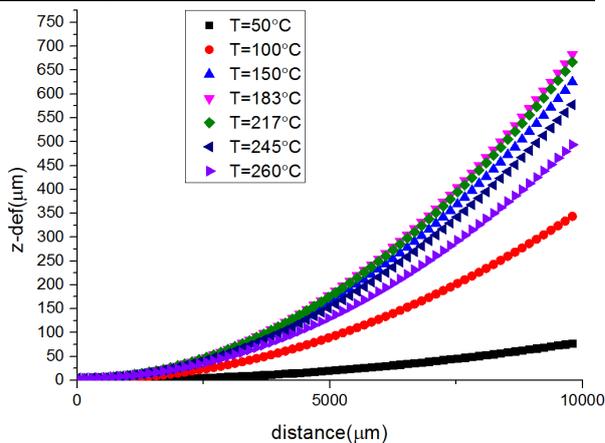
The empirical equations are expanded to predict the entire substrate deformation and the warpage behavior as shown in Fig. 13 [8].



**Fig. 12.** Z(thickness) direction displacements for all temperatures.

**Table 2.** Empirical equations.

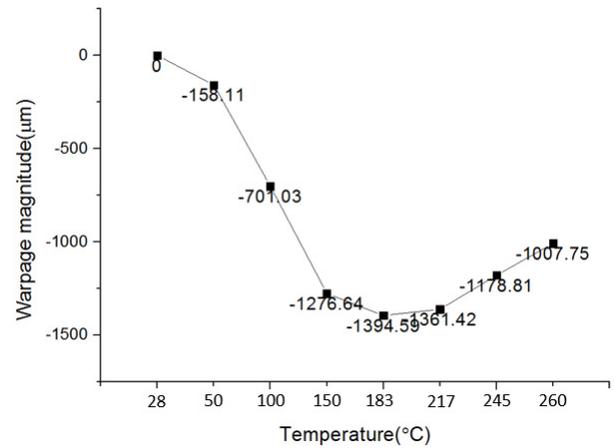
	<b>Empirical Equations</b>
T=50°C	$Z=8.07 \times 10^{-7} x^2 - 2.6 \times 10^{-5} x + 0.2$
T=100°C	$Z=3.58 \times 10^{-6} x^2 - 1.2 \times 10^{-4} x + 0.8$
T=150°C	$Z=6.50 \times 10^{-6} x^2 - 2.3 \times 10^{-4} x + 1.8$
T=183°C	$Z=7.10 \times 10^{-6} x^2 - 2.6 \times 10^{-4} x + 2.5$
T=217°C	$Z=6.94 \times 10^{-6} x^2 - 2.5 \times 10^{-4} x + 3.3$
T=245°C	$Z=5.99 \times 10^{-6} x^2 - 2.2 \times 10^{-4} x + 4.0$
T=260°C	$Z=5.10 \times 10^{-6} x^2 - 1.8 \times 10^{-4} x + 4.4$



**Fig. 13.** Curve fitting expansion to entire substrate.

Shadow morié method [9] is dependent on two diagonal lines of the substrate, and adds the highest and lowest displacement values on the two diagonals to

represent warpage magnitude, as shown in Fig. 14. Each temperature has its own warpage value.



**Fig. 14.** Transfer deformation into shadow moiré values.

## 4 Taguchi method

Taguchi method is also called Quality Engineering. It is used to decrease the experimental numbers. In this method, orthogonal arrays is selected according to factor number and level number, and discuss the influence of each control factor on quality characteristic, this method is simple and efficient [10].

During the analysis process of Taguchi methods, quality characteristic is the most important index, Taguchi method divides quality characteristic into the following three types as shown in Table 3.

**Table 3.** Quality characteristic types of Taguchi method.

<b>Quality characteristic types</b>	
Smaller-the better	Y=0
Large-the better	Y=∞
Nominal-the better	Y=m

In order to find out the main influencing factor for warpage behavior, Taguchi method is used in the finite element analysis [11, 12].

The final goal of this study is to reduce the warpage behavior as much as possible, so the maximum deformation value in thickness direction(Y) of the substrate was selected as the quality characteristic, type of Smaller-the better quality characteristic is adopted in this study.

Using the Taguchi method, the influences of the copper thickness and area occupation ratio on the thermal deformation are discussed. Four geometric variables related to copper thickness and area occupation ratio were selected as control factors as shown in Table 4, where  $H_{M1}$  and  $H_{M2}$  are the copper trace thicknesses of M1 and M2 layers,  $\rho_{M1}$  and  $\rho_{M2}$  are the copper area occupation ratio of the M1 and M2 layers.  $L_9(3^4)$  orthogonal array shown in Table 5. The corresponding simulation plan for the nine groups is shown in Table 6.

**Table 4.** Control factors and levels.

Factor	Level 1	Level 2 (Original)	Level3
A(H <sub>M1</sub> )	13μm	18μm	23μm
B(H <sub>M2</sub> )	10μm	15μm	20μm
C(ρ <sub>M1</sub> )	62%	67%	72%
D(ρ <sub>M2</sub> )	70%	75%	80%

**Table 5.** L<sub>9</sub>(3<sup>4</sup>) Orthogonal array.

Simulation \ Factor	A	B	C	D
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

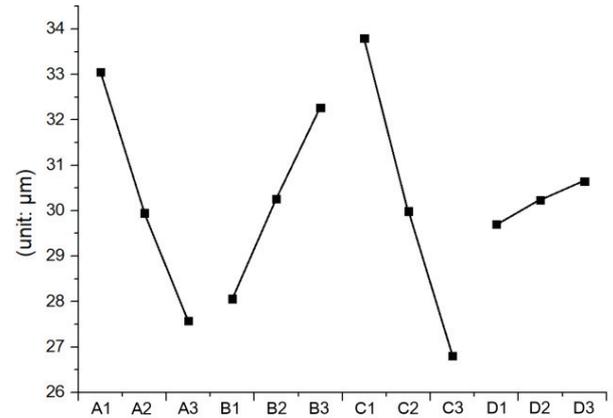
**Table 6.** L<sub>9</sub>(3<sup>4</sup>) Orthogonal array of simulation plan.

Simulation \ Factor	H <sub>M1</sub> (μm)	H <sub>M2</sub> (μm)	ρ <sub>M1</sub>	ρ <sub>M2</sub>
1	13	10	62%	70%
2	13	15	67%	75%
3	13	20	72%	80%
4	18	10	67%	80%
5	18	15	72%	70%
6	18	20	62%	75%
7	23	10	72%	75%
8	23	15	62%	80%
9	23	20	67%	70%

Through finite element, deformation value in thickness direction from simulation and the effect of each factor are shown as Table 7.

**Table 7.** Maximum deformation values for orthogonal array and the effect of each factor.

Factor \ Simulation	A (μm)	B (μm)	C	D	Y (μm)
1	13	10	62%	70%	34.03
2	13	15	67%	75%	32.95
3	13	20	72%	80%	32.18
4	18	10	67%	80%	28.06
5	18	15	72%	70%	26.13
6	18	20	62%	75%	35.67
7	23	10	72%	75%	22.09
8	23	15	62%	80%	31.69
9	23	20	67%	70%	28.95
Level 1	33.05	28.06	33.80	29.70	
Level 2	29.95	30.26	29.99	30.24	
Level 3	27.58	32.27	26.80	30.65	
Effect	-5.47	4.20	-6.99	0.94	



**Fig. 15.** Reaction diagram of factors to quality characteristic.

Reaction diagram of factors to quality characteristic is shown in Fig. 15, factor C(ρ<sub>M1</sub>), copper area occupation ratio of M1, is the most effective factor in thermal deformation. Factor D(ρ<sub>M2</sub>), copper area occupation ratio of M2, is the smallest effective factor in thermal deformation. The order of the factors is given in Eq (1) as following:

$$C(\rho_{M1}) > A(H_{M1}) > B(H_{M2}) > D(\rho_{M2}) \quad (1)$$

From Fig. 15, the best combinations for the smallest warpage behavior is A3=23μm, B1=10μm, C3=72%, D1=70%. From the tendency, it can be said that the increase of the thickness and copper area occupation ratio of M1 is better, the decrease of the thickness and copper area occupation ratio of M2 is better for decreasing the thermal warpage behavior of substrate.

## 5 Conclusions

In this paper, a finite element modelling was proposed to simulate the thermal warpage behavior of a substrate with embedded copper traces. To establish a simpler layout, an area occupation ratio is used to construct the complicated configurations of copper traces M1 and M2 layers. This concept can get a symmetrical configuration for M1 and M2. It can also simplify the complicated geometry and save a lot of simulation time. Empirical equations were also established to predict the deformation of the whole substrate.

Taguchi method was used to analyze the influence of copper traces M1 and M2. In this method, four geometric variables are H<sub>M1</sub>, H<sub>M2</sub>, ρ<sub>M1</sub>, ρ<sub>M2</sub>, analysis results for the influence in thermal deformation of four geometry factors are shown as Eq (1).

In the future, this finite element modelling will be modified. Different area occupation ratio will be set to make this model closer to the actual situation. Other parameters, such as the occupation ratio of top SR and bottom SR or the thickness of top SR and bottom SR will be optimized to get a smaller warpage of the substrate.

## References

1. M. Koide, K. Fukuzono, H. Yoshimura, IEEE, *56th Electronic Components and Technology Conference*, 1869 (2006)
2. D.H. Kim, S.J. Joo, D.O. Kwak, IEEE, *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **6**, 1667 (2016)
3. L.O. McCaslin, S. Yoon, H. Kim, IEEE, *IEEE Transactions on Advanced Packaging*, **32**, 740 (2009)
4. M.Y. Tsai, H.Y. Chang, M. Pecht, IEEE, *IEEE Transactions on Device and Materials Reliability*, **9**, 419 (2009)
5. M.Y. Tsai, C.H. Hsu, C.N. Han, ASME, *Journal of Electronic Packaging*, **126**, 115 (2004)
6. S.H. Chao, C.P. Hung, M. Chen, Y. Lee, J. Huang, G. Kao and D.B. Luh, *Microelectronics Reliability*, **57**, 101 (2015)
7. S.Y. Chiou, eThesys, *Finite Element Analyses of Copper Pillar Flip-Chip Package Processes*, (2015)
8. C. Zhu, H. Li, G. Xu and I. Luo, *Microelectronics Reliability*, **55**, 418 (2014)
9. Y.L. Guo, eThesys, *Thermo-Mechanical Deformation and Stress Analysis of Flip-Chip Ball Grid Array*, (2003)
10. H.H. Li, Gau Lih Book Co., Ltd., *Principles and Practices of Quality Design*, (2000)
11. T.S. Lan, M.C. Chiu, and L.J. Yeh, *Science Alert, Information Technology Journal*, **7**, 299 (2008)
12. H. Huh, J.H. Heo, H.W. Lee, *Int. J. Mach. Tools Manuf*, **43**, 345 (2003)