

Application of High Speed Serial Data Transmission System in Remote Sensing Camera

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Abstract. In order to meet the system needs of miniaturization, real-time, high-speed data and high reliability transmission in remote sensing camera, a high-speed serial protocol based on high-speed serial/parallel converter SerDes is proposed. For the SerDes high-speed serial data transmission chip for the physical layer, FPGA for the link layer of the communication system, design high-speed serial transmission communication protocol. Through the development of a simplified protocol for the upper user to provide a simple data interface. The system completed the data rate of 12.5Gbps point to point high-speed transmission. Verification is done by sending a pseudo-random code between boards. System work 3 hours, the measured bit error rate is less than 10^{-12} .

1 Introduction

Currently in many imaging systems and high-speed data processing systems, as the large amount of data, so the system's data transmission has high requirements. Space remote sensing instrument will get a lot of image data when working. In order to facilitate the latter part of the data processing and analysis applications, it needs for high-speed data acquisition and storage. As the amount of data is very large, the current high-speed serial differential mode is usually used for transmission[1]. This can greatly reduce the mutual crosstalk between signals and external noise interference. The adoption of new technologies to solve multi-channel and high-speed CCD / CMOS image data transmission have become an inevitable trend. High-speed differential serial bus interface technology to improve data transmission bandwidth becomes effective solution[2].

This paper introduces a new type of high-speed serial-to-parallel converter in remote sensing camera applications and SerDes high-speed serial data transmission chip Redundant XAUI Transceiver. According to the characteristics of the project designed the data transmission system of new SerDes high-speed serial data transmission chip.

2 Introduction to SerDes

The SerDes high-speed serial data transmission chip is a new high-speed transceiver device based on Serializer /DESerializer technology from Texas Instruments Inc which enables error-free transmission on 80-inch long standard backplane lines. Dual point-to-point serial transfer rate of up to 12.5Gbps. SerDes high-speed serial data transmission chip is using VML differential signal which has good anti-

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jamming capability. It uses the self-synchronous communication with clock and data recovery technology instead of synchronous transmission of data and clock. This can resolved signal and clock offset problems. In addition, the serial communication technology to take full advantage of the transmission channel capacity, reduce the number of connector pins required and the number of chip peripheral pins. The equipment and cable wiring is more simple, and the system is more resistant to interference. SerDes high-speed serial data transmission chip is flexible, redundant XAUI serial transceiver, as shown in Figure 1, SerDes has A, B two identical XAUI port, with self-backup function.

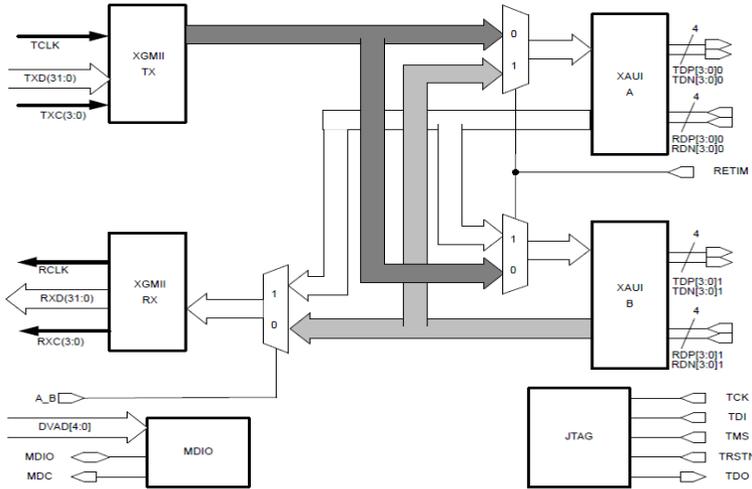


Figure 1. SerDes high-speed serial data transmission chip

The new SerDes uses full-time duplex point-to-point high-speed serial signal communication protocol. The parallel data transmitter and receiver are 4 channels. Each channel is 8 bit wide with a total of 32bit as a transmission unit.

3 System composition and processing flow

3.1 Design

The system is designed to achieve high-speed serial CCD image data transmission which mainly for the satellite payload and back-end data processing equipment between the communication interface. The high-resolution image data acquired from the satellite payload is transmitted to the back-end data processing module. The output of the SerDes is mainly for data transmission to complete the function of high-speed serializer[3].

In this paper, high-speed serial data transmission structure to replace parallel which can greatly reduce the number of interconnection lines and line interference. The number of the corresponding connector terminals and the transmitting and receiving terminal chips are greatly reduced, and the whole system is miniaturized in accordance with the current development trend. The parallel data loaded into the transmitter is transmitted to the receiver via a serial channel, which can be a coaxial cable, an impedance-controlled backplane, or a fiber-optic link [4-5].

SerDes high-speed serial data transmission interface consists of three parts, including the transmitter, transmission cable and receiver. The transmitting end includes transmitting data processing circuit, SerDes send circuit, crystal, clock management, electrical connectors and other parts. The receiving end includes receiving end data processing circuit, SerDes receiving circuit, crystal, clock management, electrical connectors and other parts.

SerDes interface using serial transmission mode, the clock frequency is 156.25MHz ± 200ppm. In the receiving end need to ensure that REFCKJ and TCLK is the same source clock, so pay special

attention to the clock signal design. The clock management is used to provide a reference clock to the SerDes. The clock management is a high performance, low phase noise and low clock skew synchronizer that synchronizes the frequency of a voltage controlled crystal on a circuit board to an external reference clock. System block diagram is shown in Figure 2.

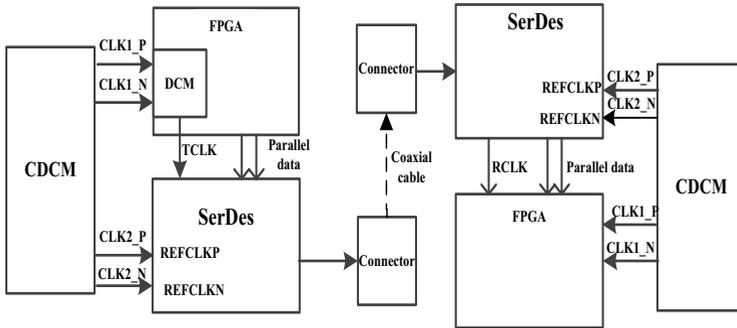


Figure 2. system block diagram

3.2 Transfer Protocol

SerDes high-speed serial data interface using point-to-point simplex communication. The data is passed on the channel as a data frame. In order to ensure that the data frame in the protocol channel in the correct transmission, you must transfer some control characters in the channel, and design a certain transmission protocol. The manner of this agreement is: After power-on or reset, both sides are out of synchronization (It requires the transmitter to reset, the receiving end to ensure that the receiver is already in the state). The sending end sends a sync character (idle character) for one millisecond. The system completes the synchronization process. After 1 millisecond, the transmitter starts the transmission of the data frame. The transmitting side is required to transmit not less than a certain number of synchronization characters before the transmission of each frame data is completed and before the transmission of the next data frame is started. And then send the next frame of data, the loop until the camera stops working. If the receiver side in the frame data transmission process out of sync, rely on data of the synchronization characters to re-establish the synchronization between the transceiver relations.

This protocol specifies that the frame data consists of frame header (S), frame end (T) and data. The start character of frame data is S (XGMII side is 0xFB), can only appear on Lane0. The termination character is T (0xFE on the XGMII side) and can appear on any Lane. The format is shown in Figure 3:

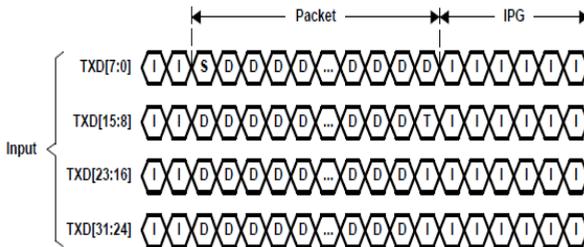


Figure 3. frame data format

The valid control characters are shown in table 1: The frame header is defined as: 07070707FFFFFFFFB (64-bits converted to DDR 07070707, FFFFFFFFFB); The frame tail is defined as: 070707FD07070707 (64-bit converted to DDR 070707FD, 07070707); Idle characters are defined as: 0707070707070707;

Table 1. Valid control characters

Primitive Description	K code	Control word TXC(3:0)	Data TXD[X:X-7]
SOP(S)	K27.7	FB	1
EOP(T)	K29.7	FD	1
Idle	K28.0	07	1
Valid characters	00~FF	00~FF	0

3.3 System Workflow

The SerDes high-speed serial data transmission system is first to complete the reset operation, and then enter the Loop-Back self-test mode. If the link has been synchronized to enter the next step, otherwise it has been in self-test state. After the link is synchronized, send the data sync word and receive the data sync word at the same time. The working process is in Figure 4.

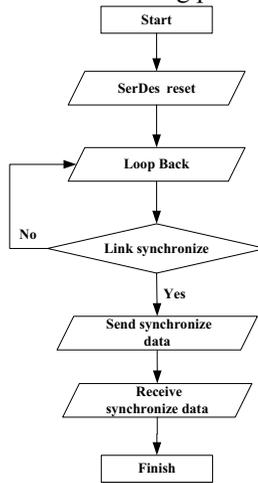


Figure 4. system workflow chart

The FPGA as the control center of high-speed serial transceiver is adjusting the control word of SerDes to configure its work state. Control word as shown in the Figure 5.

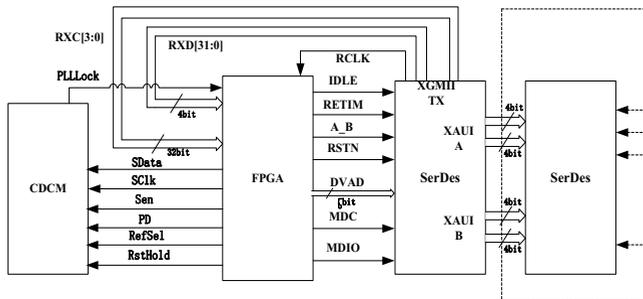


Figure 5. high-speed serial data transmission system

Among them: RSTN (Chip Reset) is a SerDes reset signal that requires at least 10us reset time. RETIM (Re-Timer Mode Enable) signal is pulled low to configured SerDes as redundant mode. IDLE signal is pulled low to mapping XGMII TX data of XAUI A and XAUI B port at the same time. By configuring A_B to choose output port. By configuring DVAD(0) to choose DTE (Device Address) or PHY(Physical Address). Whether SerDes working status is correct is judged by setting the read and write different address register values with MDIO. The read and write reference clock is provided by

the MDC (Management Data Clock). Specific timing requirements are shown in Figure 6. Where t_p is a minimum of 400ns, t_{su} is 10ns minimum, and t_h is 10ns minimum. So the frequency of MDC is 512ns.

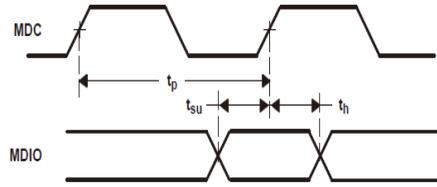


Figure 6. MDIO Read/Write Timing Diagram

First, SerDes is set to Loop Back mode as self-test mode. By writing address 0x0000 to data 0x6040, set this register to 0x6040 to check if SerDes has completed the function of spontaneous self-collection. If Self-test mode is correct, read 0x0008 address register data, check the transceiver link whether is normal. If the return value is 0x8000, then the link is normal, the link has been synchronized, if the return value of 0x8C00 said that the transceiver is not normal, if the return value of 0x8400 said the receiving link is not normal, if the return value of 0x8800 Indicates that the sending link is not working properly.

Through the state machine to control the register of read and write operations are shown in Figure 7. From the simulation waveform can be seen, STATE (1) and MDIO (1) for write register address, STATE (2) and MDIO (2) for write register data, STATE (3) and MDIO (3) for read register address. The actual application by reading and writing different address register values to check the working status of SerDes.

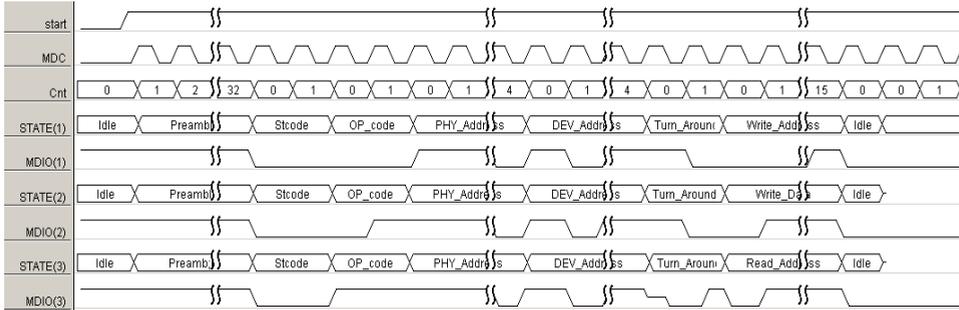


Figure 7. Data Input Timing Diagram

After checking the link is correct, data processing circuit will send parallel data with frame start and end. The SDR parallel data is converted to DDR data via ODDR, and the clock is sent to SerDes. The transmission data timing is shown in Figure 8.

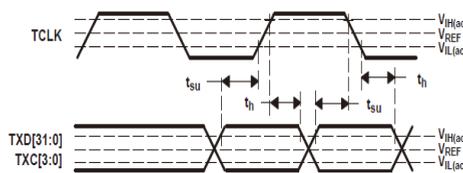


Figure8. Send clock timing diagram

Where t_{su} is at least 480ps and t_h is at least 480ps. It sends data at the sending clock signal along the transition edge. That is send the clock transition edge along the data center, the effective data in the clock after the shortest time to keep 480ps, the data valid to the clock transition edge needs at least 480ps to settle. So the frequency of tclk is 156.25M and the change frequency of data is 312.5M.

The receiver reads the data by receiving the SerDes recovery clock RCLK. The receiving circuit performs data extraction on the received data frame according to the alignment character. It converts 32-bit DDR data into 64-bit SDR data, remove the frame start and end, extract the valid data unit, and give the data flag. The received data timing is as shown in Figure 9.

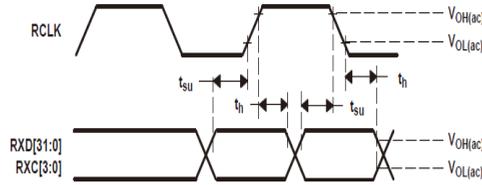


Figure 9. Restore the clock timing diagram

Where t_{su} is at least 960ps and t_h is at least 960ps. The clock edge of the receive clock signal reads the data, that is, the receive clock transition edge is aligned with the data center. Valid data is kept at a minimum of 960ps after clock hopping, and data settling time to clock hopping is as short as 960ps. SerDes's send clock and reference clock must be homologous clocks, so SerDes restores the clock based on the clock manager to give the reference clock according to SerDes which is $156.25\text{MHz} \pm 200\text{ppm}$.

4 Testing and verification

The reliability of the system is verified by testing the bit error rate by connecting the system to the BERT. In the test the sending end sends pseudo-random code, the receiving end monitor whether the received data is sent to the data. In the receiving end of the data processor FPGA for error counter, the error flag bits are counted, in order to statistics error rate.

System test 3 hours and sending clock is 156.25MHz. Receiver error flag bit is always high, indicating that the pseudo-random number sent and received the same, there is no error code.

5 Conclusion

In order to meet the mass data transmission requirements of high resolution camera, a SerDes serial transmission method is proposed. The system not only greatly reduces the complexity of high-speed image data transmission process, but also to ensure the reliability of signal transmission. Verification of the system compared to the traditional SerDes data transmission system transmission efficiency is higher, the transmission capacity increased by 1 times the transmission rate increased to 12.5Gbps. Single-chip new SerDes with A, B two redundant interface, comes with backup function, effectively saving space. Compared with the traditional serial conversion system, not only improve the transmission rate, but also reduces the cost of space. The test shows that the system is stable and reliable.

References

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