

Power factor corrector with a high-order harmonics filtering function

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Abstract. The article presents an original method and a control system of the active power factor corrector (PFC), which allows integrating the function of a parallel active filter of high-order harmonics into it. This makes it possible to reduce the total harmonic distortion of the grid voltage at the point of connection of the PFC with the proposed control system, thereby improving the working conditions of other electrical equipment in this grid. The presented control method is applicable to all PFC topologies employing direct control of the input currents.

1 Introduction

The adverse effects of harmonics on electrical power systems are well known [1, 2]. Harmonics current generated by any non-linear load flows from the load into the power system. These harmonic currents degrade the power system performance and reliability and can also cause safety problems. Harmonics need to be clearly located, sources identified and corrective measures taken to prevent them.

Introduction of modern electromagnetic compatibility standards that limit harmonic currents emission (IEC 61000-3-2, IEC 61000-3-4, IEC 61000-3-12) determines the intensive development of technical means that prevent deterioration of the power quality due to the presence of harmonics. These means are passive harmonic filters, harmonic mitigating transformers, active power filters [3-5], power quality conditioners [6, 7], unified [8] and interline [9] power flow controllers. Another way to improve electromagnetic compatibility of power supplies is to equip them with power factor correctors (PFC).

Most widespread among single-phase systems is the PFC based on a boost converter (the so-called Boost-type PFC, Fig. 1).

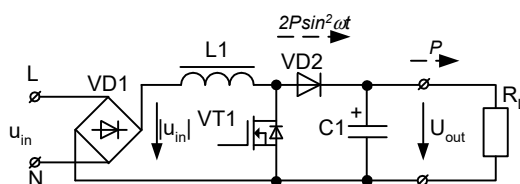


Fig. 1. Typical schematic of the single-phase boost-type PFC power stage.

The vast majority of such PFC behave as a linear active resistance in relation to the supply network (Fig. 2a). There is also a small number of PFC (for

example, based on the M81012FP control chip from Mitsubishi) [10], behaving as sources of the sinusoidal current with fundamental frequency (Fig. 2b).

In both cases, the PFC does not have an active influence on the mains voltage spectrum (and in the case shown in Figure 2b, the voltage total harmonic distortion THD_U may even increase due to a voltage fundamental amplitude decrease).

As modern networks are flooded with non-linear loads, the problem of compensation of their negative impact on power quality arises.

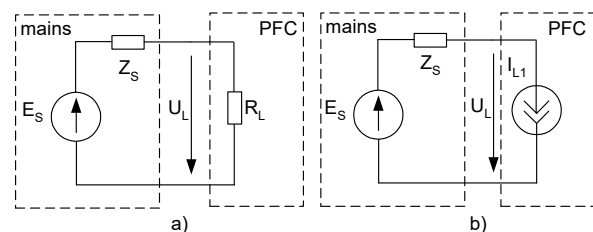


Fig. 2. PFC emulating: a) active resistance; b) sinusoidal current source.

As for today, there is a large number of electric loads that use intermediate conversion of alternating supply voltage to DC (switching power supplies, welding inverters, variable frequency drives, etc.). Typically, this conversion is carried out by means of a diode bridge and a capacitive filter. The input current of such a load has high content of odd harmonics, mainly 3rd and 5th, and typical power factor (PF) lies in the range of 0.5 to 0.7. The presence of a large number of such loads leads to a distortion of the mains voltage waveform, an overload of the neutral wire, a significant deterioration in the operating conditions of power supplies, especially with thyristor regulators with phase angle control, etc.

The negative impact of the non-linear loads on the mains voltage can be sufficiently reduced by means of installing the active power filters (APF) and/or

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equipping the loads with power factor correctors. These measures allow bringing the power quality parameters up to modern requirements.

At present, APFs are built using four-quadrant inverters. This is dictated by the need to provide a bi-directional instantaneous active power flow and leads to a complication of the power stage and its control system.

The power stage of the PFC, in its turn, is optimized for operation only with positive instantaneous active power (in the 1st and 3rd quadrants), which makes it impossible to use classical APF control algorithms for it.

In addition to the power stage, parallel APF usually requires installation of current sensors for compensated non-linear loads. However, the need for current sensors can be eliminated by operating the parallel APF inverter in a voltage source mode, as shown in [11].

2 Proposed PFC control strategy

The authors proposed the PFC [12] with a control system which allows for integration of parallel APF functions into it while ensuring regulation of the PFC output voltage, working with a positive input instantaneous active power, and limitation of the PFC input current. The control system operates in the conditions of absence of information about the currents of non-linear loads connected to the mains.

The essence of the idea is to change the algorithm of the PFC control system in order to reduce the emulated input resistance.

For this purpose, the input current of the PFC $i_L(t)$ is formed in accordance with the equivalent circuit shown in Figure 3.

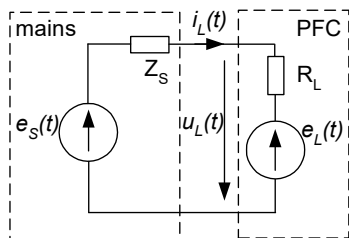


Fig. 3. Proposed PFC equivalent schematic.

As it was said before, the PFC with respect to mains behaves like an active resistance R_L , but now it has its own EMF $e_L(t)$, which contains only the fundamental mains frequency in its spectrum.

The source of the EMF $e_L(t)$ is synchronized with the mains voltage by means of phase locked loop (PLL):

$$e_L(t) = E_R \sin(\omega t), \quad (1)$$

where ω – mains voltage angular frequency; E_R – amplitude reference.

In this case, the input current of the PFC is

$$i_L(t) = [u_L(t) - e_L(t)]/R_L, \quad (2)$$

where R_L is the emulated input resistance of the PFC.

The magnitude of the E_R amplitude reference is chosen so that the instantaneous active power of the PFC

is always positive: $i_L(t) \cdot u_L(t) > 0$ (the condition of the correct operation of the PFC power stage, see above), which allows using the developed control method for almost all existing power stage topologies of active PFC with direct input current control.

The value of R_L is determined from the power balance condition (the necessary condition for regulating the PFC output voltage).

$$(\omega/2\pi) \cdot \int u_L(t) \cdot [u_L(t) - e_L(t)/R_L] dt = P, \quad (3)$$

where P is the power drawn from the network.

E_R and R_L signal conditioning circuits should not allow rapid changes in these signals, otherwise the performance of the system will deteriorate.

In comparison with the conventional PFC (Fig. 2a), the R_L value obtained for the same output power will be smaller. Thus, because of the reduced input resistance, the PFC will have an increased shunting effect for the high-order harmonics currents, similar to parallel APF.

The block diagram of the control system that implements the developed method is shown in Figure 4.

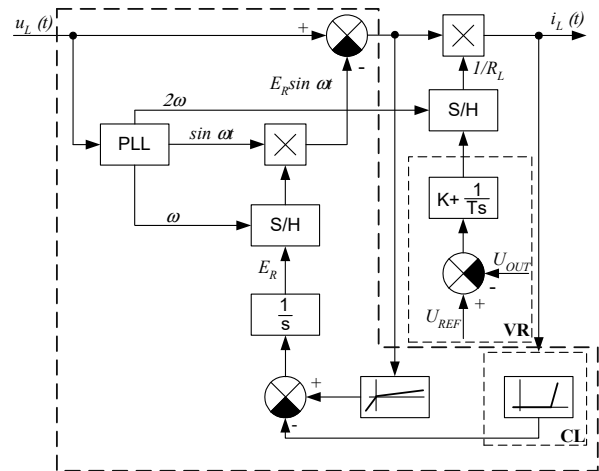


Fig. 4. Block diagram of the proposed PFC control system.

The reference signal of the fundamental harmonic of the mains voltage is obtained using the PLL (Fig. 4) and together with the amplitude reference (E_R) is fed to a multiplier whose output is connected to an adder that generates a difference signal. This signal is fed to the second multiplier, which works in conjunction with the PI controller of the PFC output voltage (voltage regulator VR, Fig. 4), and generates a PFC input current reference signal $i_L(t)$.

The E_R signal is generated by a local negative feedback circuit comprising a stage with a transmission coefficient that is switched depending on the polarity of the input signal, and an integrator. The time constant of the E_R circuit must significantly exceed the mains voltage period (i.e., E_R should not vary significantly during the period).

The PFC input current limiter (CL, Fig. 4) with the threshold stage reduces the E_R amplitude reference in case of an unacceptable increase in the PFC input current. Since this current limiter has a delay due to the E_R integrator, the high-speed hardware current limitation

must also be performed directly in the power stage control circuits.

To prevent changing of the emulated resistance R_L and amplitude reference E_R during the mains period, Sample-and-Hold (S/H) stages synchronized with the mains voltage are used in control system. Thus, in the E_R amplitude reference signal, all harmonics of the mains frequency are suppressed, as a result of which it contains only a slowly varying DC component, which is necessary for the correct operation of the PFC. Similarly, in the U_{OUT} signal, all even harmonics of the mains frequency are suppressed, which eliminates the influence of output voltage ripple on the spectrum of the PFC input current [13].

3 Simulation

Figure 5 shows the results of simulating the work of the developed PFC control algorithm under conditions of a distorted mains voltage (the secondary side voltage of one of the Mariupol city substations: $U_{RMS} = 187$ V, $THD_U = 9$ %, with the 3rd harmonic coefficient of 8.2 %). The PFC output power is $P = 2$ kW. Simulation gives the developed PFC power factor $PF_{PFC} = 0.818$.

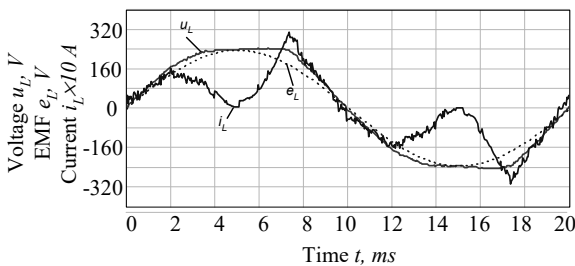


Fig. 5. Simulation results of the input current (i_L) of the proposed PFC under distorted mains voltage waveform (u_L).

It should be noted that the voltage quality parameters of this substation do not comply with modern power quality standards at least due to high THD_U .

In the mains voltage (u_L), high-order harmonics are expressed due to the presence of a large amount of nonlinear loads with uncontrolled single-phase rectifiers in the power supply network. The PFC reacts on this distorted voltage by the appearance of high-order harmonics in its input current (i_L) with the phases of these currents being opposite to the phases of the currents that caused distortion of the voltage waveform.

The analysis of the PFC input current spectrum shows a significant level of the high-order harmonics, significantly above the level of the harmonics in the mains voltage (for the given case, $THD_U = 9.1$ %, $THD_I = 82.5$ %). This is caused by the developed PFC control system attempt to increase the active power transferred by high-order harmonics. This fraction of the power can be defined as:

$$P_H^* = 1 - U_{1m} \cdot (U_{1m} - E_R) / (2R_L \cdot P), \quad (4)$$

where U_{1m} is the amplitude of the fundamental harmonic of the mains voltage.

Calculation by formula (4) for the given case shows that 7.9 % of the PFC input power is provided by higher voltage harmonics. While with a PFC emulating purely active load (as shown in Fig. 2a), this fraction will be determined as

$$P_H^* = 1 - 1 / (1 + THD_U^2), \quad (5)$$

which, for the case under consideration, is only 0.8 %, and for the case of PFC shown in Fig. 2b, the active power transferred on the high-order harmonics is zero.

The effect of increasing the power fraction of high-order harmonics is associated with a decrease in the PFC emulated input resistance (R_L). In the case under consideration, the developed PFC operates with parameters $E_R = 235$ V, $R_L = 2.03$ Ohm. At the same time, the conventional PFC (Fig. 2a) would have $R_L = 17.48$ Ohm under similar conditions.

Figure 6 shows an example of the effect of replacing the conventional PFC (Fig. 2a) with the PFC employing the described control system (Fig. 3). Replacement of the conventional PFC (Fig. 6a) with a PFC control system, developed by the authors (Fig. 6b), leads to an increase in the total power factor of the system: $PF_2 > PF_1$.

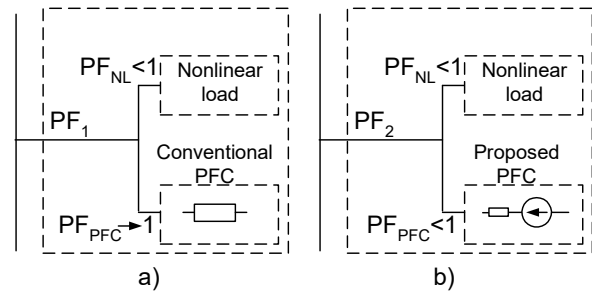


Fig. 6. Effect of using the proposed PFC with nonlinear load: $PF_2 > PF_1$.

Thus, the power factor of the system "non-linear load + developed PFC" will be higher than that of the "non-linear load + conventional PFC" system, despite the fact that the power factor of the developed PFC will be noticeably below unity. This effect is explained by the fact that in the case shown in Fig. 6b, a part of the high-order harmonics of the non-linear load current is supplied by the PFC, and not by the mains.

In case of a "clean" mains voltage (with an insignificant level of high-order harmonics), the operation of the developed PFC is completely analogous to the conventional one, i.e. its input current will contain only the fundamental harmonic component.

4 Experiments

For experimental verification of theoretical results, a modified PFC based on the MC33262 control IC was created (Fig. 7). The instantaneous mains voltage processing circuit of the PFC has been modified to implement the active filtering function with the possibility of switching it off.

The processing of the mains voltage signal was carried out using a single-chip microcontroller

ATTiny13; the generation of a current reference signal for the MC33262 was performed by filtering the microcontroller-generated pulse width modulated (PWM) signal using the low settling time filter developed by the authors [14]. The appearance of the signal processing unit is shown in Figure 8.

Measurement of power quality parameters and oscillography of voltages and currents was performed using the power quality analyzer developed by the authors [15].

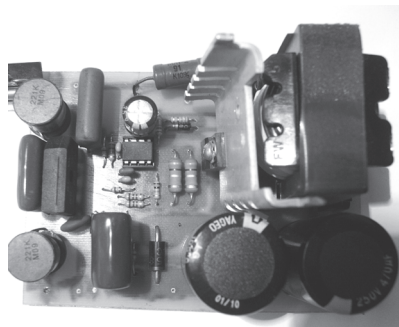


Fig. 7. Experimental PFC prototype.

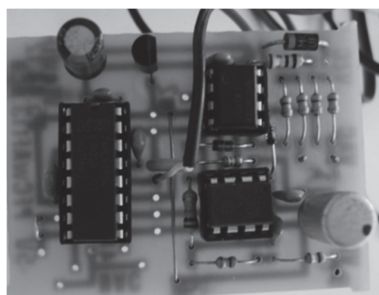


Fig. 8. Signal processing unit for an experimental PFC.

The PFC operated together with a nonlinear load, which was presented by a bridge rectifier with a 330 μ F smoothing capacitor, loaded with an active resistance and consuming 100 watts at a mains voltage of 193 V_{RMS} .

The output power of the experimental PFC was 140 – 160 W.

Figures 9 and 10 show the oscillograms of the mains voltage and current when the active filtering function is turned off and on, respectively. For the convenience of representation, the signals are normalized to their amplitudes.

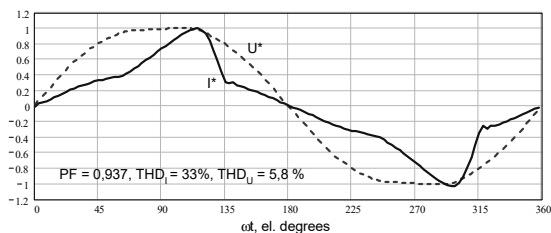


Fig. 9. Mains voltage and current with PFC emulating active resistance.

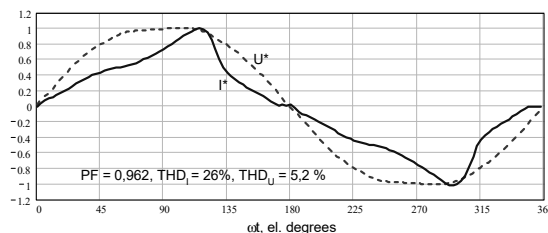


Fig. 10. Mains voltage and current with PFC in active filtering mode.

As can be seen from the presented oscillograms, activation of the active filtering function in the PFC resulted in an increase in system PF from 0.937 to 0.962; the reduction of THD_I from 33 % to 26 % and the reduction of THD_U from 5.8 % to 5.2 %. These results confirm the operability of the described control method of the active PFC.

Figures 11 and 12 show the oscillograms of the mains voltage and the input current of the experimental PFC when operating under conditions of a “clean” mains voltage (Fig. 11) which is simulated using an apparatus described in [16], and under conditions of a “real” mains voltage (Fig. 12).

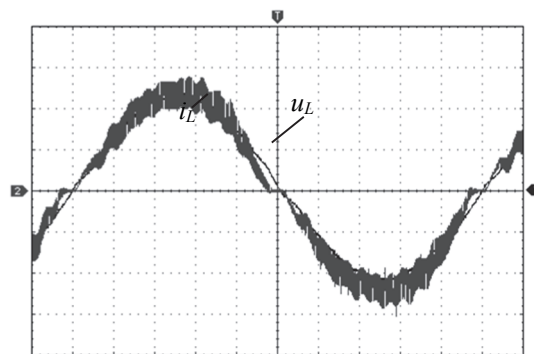


Fig. 11. Mains voltage (u_L) and input current (i_L) of the proposed PFC under “clean” mains voltage (THD_U is less than 2 %).

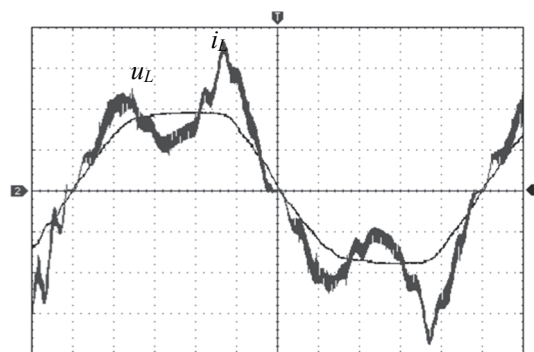


Fig. 12. Mains voltage (u_L) and input current (i_L) of the proposed PFC under “real” mains voltage (THD_U is about 6 %).

In case of low THD of the mains voltage, the proposed PFC works in the same way as conventional PFC emulating active resistance (Fig. 2a). But in case of distorted mains voltage, the proposed PFC starts

absorbing harmonic currents in such a way as to lower voltage distortion. In Figure 12, flat-topped voltage waveform appears due to the presence of loads drawing current near the peaks of voltage. Unlike these loads, proposed PFC reacts to such voltage distortion by reducing its current draw near the peaks, thus lowering overall system current THD. A good agreement with the simulation results can be seen (waveforms shown in Figure 12 and Figure 5).

5 Conclusion

Thus, the PFC with the described control system allows the functions of a current sensorless parallel active filter to be partially integrated into it by increasing the ability to absorb high-order harmonic currents generated by the non-linear loads present in the power network. This leads to improving the spectral composition (reducing THD) of the mains voltage. The proposed control method can be used for practically all known PFC topologies with direct control of the input current.

A similar method and control system can be used for 3-phase active PFC, as well as for direct conversion type switchmode power supplies, in which there is a possibility of direct control of the input currents. In this case, one should only take into account that in the case of a three-wire connection to a three-phase network, it is necessary to filter out the zero sequence component of the phase voltages before processing them in accordance with the algorithm described above.

The use of electric apparatus equipped with PFC having the functions of high-order harmonics filtering will ease the achievement of compliance with the standards of electromagnetic compatibility of technical equipment, improve the mains electric power quality and improve the working conditions of other equipment connected to the same power supply network.

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