

3D Simulation and Modeling of Ultra-fast 3D Silicon Detectors

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Abstract. 3D detectors with very small electrode spacing can provide ultra-fast detection due to their extremely small charge collection time. Since the detector full depletion voltage and charge collection time are independent to the detector thickness, ultra-fast 3D detectors can be made relatively thick (or not too thin, $\sim 200\ \mu\text{m}$) to ensure a large signal. The results of the 3D simulations and modeling of 3D silicon detectors with very small electrode spacing and relatively large thickness will be shown in this paper. The column spacing LP is in the range of $5\ \mu\text{m}$ to $10\ \mu\text{m}$. At a bias voltage of only a few volts, the electric field in the detector can be large enough to ensure the carrier saturation drift velocity in most volume of the detector, and the detector charge collection time there can be as short as 10^3 of ps. In this paper, we will analysis the simulated electrical characteristics of this detector structure through systematic 3D simulations using the Silvaco's TCAD tool. Profiles of detector electric potential and electric field will be presented. We will investigate the region of low electric field (the "slow region") in the detector. We will also exam whether the detector reach the breakdown condition at operation voltages suggested in this work.

Keywords. 3D simulation, Ultra-fast, 3D silicon detector, Electric field

1 Introduction

In the middle 1990's, S.I. Parker and his colleagues proposed a structure of solid-state radiation detectors using a 3D array of electrodes that penetrate into the detector's bulk [1]. In recent years, researchers of 3D detectors have mainly focused their efforts on improving detector radiation hardness by proposing various 3D structures as tracking detectors for the high luminosity upgrade of the Large Hadron Collider (HL-LHC) [2-8]. Examples of them are 1) In 2008, a non-fully penetrating, dual-column structure was proposed [6], with an electrode spacing of $50\ \mu\text{m}$; and 2) a double-side, dual column structure [7]. In 2010, it was pointed out that in future development for detectors irradiated up to $1 \times 10^{16}\ \text{n/cm}^2$, to fully depleted a dual-column 3D detector with a reasonable bias, the columns' spacing should be further reduced to $30\ \mu\text{m}$ [8].

In this work, we further reduced the column spacing to obtain ultra-fast detectors with reasonable signal size. An all column electrode 3D silicon detector with very small electrode spacing and a thickness of $200\ \mu\text{m}$ is shown here in Figure. 1. For simplicity, we chose the etch-through columns in the simulations, which will not affect the conclusion obtained in this work about the property of ultra-fast charge collections of this type of detectors. In practice, the etch-through detectors can be realized by using a support wafer or SOI. The column spacing is chosen in the range of $5\ \mu\text{m}$ to $10\ \mu\text{m}$. As we will show, at a bias voltage of only a few volts, this structure's charge collection time can be as fast as 10^3 of ps. We undertook full 3D simulations of dual-column 3D detectors with the

Silvaco DEVICE3D package within ATLAS [9].

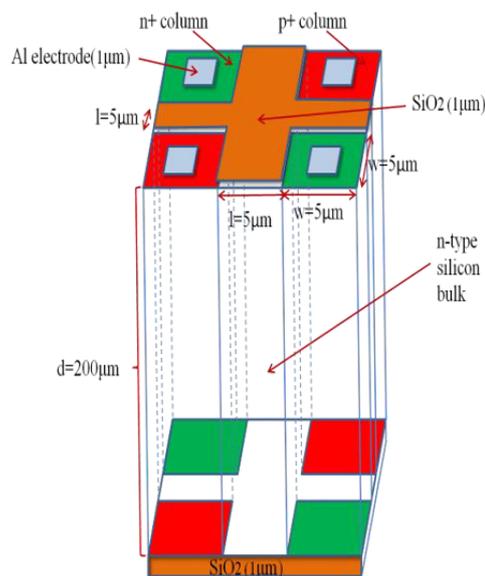


Figure 1. 3D device structure in square shape.

2 The device description and 3D simulation

Figure. 2 is the cell of the detector simulated in this work. This structure consists of two n-type- and two p-type-doped columns on n-type substrate with an initial phosphorous doping concentration of $1 \times 10^{12}\ \text{cm}^{-3}$. The width of all columns is $5\ \mu\text{m}$, which can be realized with

today's new etching technology on wafers with relatively thin thickness ($\cong 200 \mu\text{m}$). The distance between the electrodes is $5 \mu\text{m}$ or $10 \mu\text{m}$. The doping concentrations of the columns are $1 \times 10^{19} \text{cm}^{-3}$. (boron for p^+ columns and phosphorous for n^+ columns, respectively). Depths of the n^+ column electrode and the p^+ column electrode are all $200 \mu\text{m}$, the same as the detector thickness. With improved processing technology at Fondazione Bruno Kessler (FBK), Trento, Italy, columns with $5 \mu\text{m}$ width can be etched up to $200 \mu\text{m}$ using their Deep Reactive Ion Etching system with aspect ratio up to 30:1 [10]. For a detector with column spacing of $10 \mu\text{m}$, collection electrodes can be read out using a bump bonding technology of $10 \mu\text{m}$ bumps. Although technically bump bonding technology of $10 \mu\text{m}$ bumps may not be used for a detector with column spacing of $5 \mu\text{m}$, with future improvements of bump bonding technology, it may also be realized. We therefore went ahead to simulate this extreme situation for future applications. Anode and cathode electrodes are formed by covering $1 \mu\text{m}$ aluminum on n^+ and p^+ columns on the top side of the detector. Other parts of the top side (area between electrodes) and the entire area of the bottom side of the detector are covered by $1 \mu\text{m}$ thick SiO_2 layers. Figure 2 is the top view (although it looks up) of square column of columns spacing in $10 \mu\text{m}$ and $5 \mu\text{m}$ simulated using Silvaco's 3D TCAD tool. The aim of the numerical simulations is to investigate the minimum bias voltages needed for carriers, generated by incident particles/photons, to reach the saturation drift velocity in the most part of the detector volume. Detector depletion voltages will also be determined.

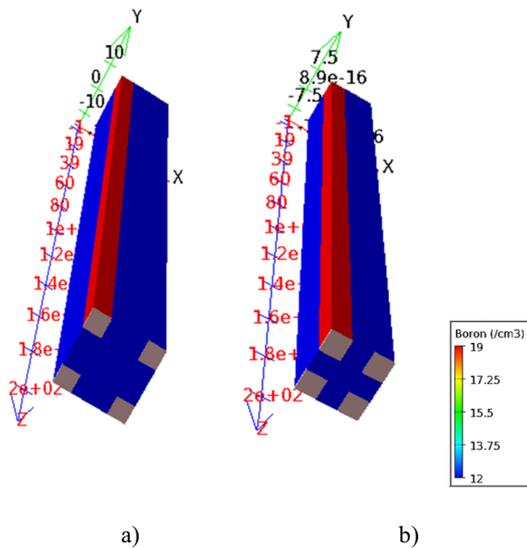


Figure 2. Detector structure simulated in this work with a) $10 \mu\text{m}$ and b) $5 \mu\text{m}$ electrode spacing.

3 Detector electrical characteristics

Before the full 3D simulation, let us first estimate the minimum bias voltage needed to reach the carrier saturation drift velocity in the detector. Carrier (electrons here) drift velocity can be written as:

$$v_{dr} = \frac{\mu_e E}{1 + \frac{\mu_e E}{v_s}} \quad (1)$$

Where v_{dr} is the drift velocity of electrons induced by the incident particle, v_s is the saturation velocity for electrons, and E is the electric field in the detector.

To reach saturation velocity, $v_{dr} = v_s = 1 \times 10^7 \text{cm/s}$, we must have $E \gg \frac{v_s}{\mu_e}$. From $\mu_e = 1450 \text{cm}^2/\text{Vs}$, we can get $E \gg 10^4 \text{V/cm}$. So we chose the minimum electric field to reach the carrier saturation drift velocity as 10^4V/cm . When the carrier saturation drift velocity is reached, the charge collection time is then $t_c = L_p / v_s$.

The relationship between the average electric field E and the bias voltage V can be written as: $E = \frac{V}{L_p}$. Then we have:

$$\frac{V_{min}}{L_p} = \frac{v_s}{\mu_e} \quad (2)$$

where V_{min} is the minimum voltage needed for carriers to reach the carrier saturation drift velocity:

$$V_{min} = \frac{v_s}{\mu_e} \times L_p \quad (3)$$

For example, for $L_p = 5 \mu\text{m}$, V_{min} is about 3.5 volts, and the charge collection time is about 50 ps. Similarly, for $L_p = 10 \mu\text{m}$, V_{min} is about 7 volts. The charge collection time is about 100 ps. While for $L_p = 20 \mu\text{m}$, V_{min} is 14 volts, and the charge collection time is about 200 ps, etc. In the full 3D simulations of this work, we carried out simulations around these estimated minimum voltages, and use the electric field value of 10^4V/cm to determine if most of the detector volume reaches the carrier saturation drift velocity condition. On the other hand, our full 3D simulations of the detector can verify what we calculated above. Profiles of simulated detector electric potentials, electric fields will be shown below. Detector full depletion voltages are obtained from simulated electric potential and electron concentration profiles.

To illustrate the detailed electric potential and electric field profiles in our 3D Si detectors, we made 2D cut planes along the detector thickness (Z -direction, at $z=103 \mu\text{m}$), as depicted in Figure. 3 to Figure. 8. Figure. 3 and Figure. 4 are the electric potential profiles of two structures with different electrode spacing. We put negative voltages on cathode electrodes, while zero bias on anode electrodes. Bias voltages are -5 and -8 volts for

Figure. 3 and Figure. 4, respectively. As one can see in Figure. 3, the potential near p^+ electrodes is about -5 V, and that near n^+ electrodes is 0 V. The potential at the center of the detector cell is -2.5 V. These potential distributions clearly define a saddle shape potential, with zero electric field at the center regardless of what value the bias voltage is. Similar conclusions can be easily obtained from Figure. 4, where the potential is -8 V near p^+ electrodes and that near n^+ electrodes is 0 V.

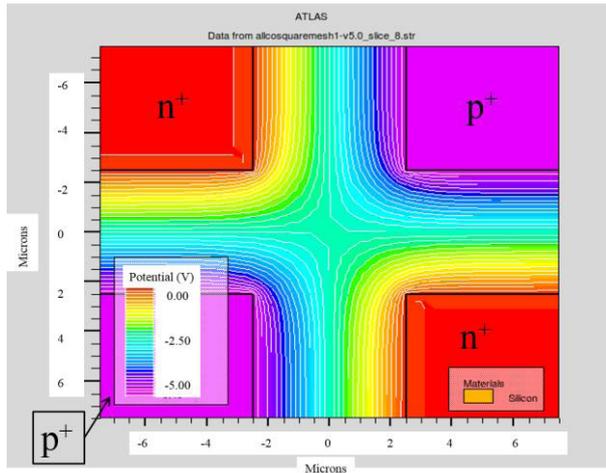


Figure 3. Electric potential profiles of detector with a column spacing of 5 μm . The bias voltage is -5 volts.

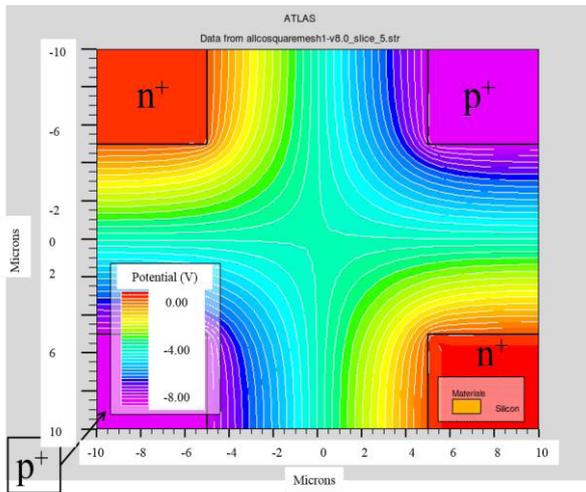


Figure 4. Electric potential profile of a detector with a column spacing of 10 μm . The bias voltage is -8 volts.

From simulations of the electric field profiles, as shown from Figure. 5 to Figure. 8, we can observe that in the majority regions of detectors, the electric field already reaches to 10^4 V/cm when the absolute value of bias voltage V is larger than 4 and 8 volts for $L_p = 5 \mu\text{m}$ and $L_p = 10 \mu\text{m}$, respectively. For example, as shown in Figure. 5, where L_p is 5 μm and bias voltage V is -4 volts with the maximum electric field (or the upscale of electric field display for better clarity) shown as 1.5×10^4 V/cm, the electric field in regions between p^+ and n^+ electrodes is larger than 10^4 V/cm. As we calculated above, we can therefore get a minimum carrier drift time of about 50 ps in these regions of the detector at a bias voltage of $|V| \geq 4$ V for $L_p = 5 \mu\text{m}$. As shown in Figure. 6, when the bias

voltage goes to -6 volts, the electric field reaches 2×10^4 V/cm in regions between p^+ and n^+ electrodes of the detector, which will further guarantee the carrier saturation drift velocity condition. Shown in Figure. 7-8 are simulated electric field profiles at two different bias voltages for a detector with electrode spacing of 10 μm ($L_p = 10 \mu\text{m}$). Similarly, as shown in Figure.7 and Figure.8, the electric field reaches 10^4 V/cm in regions between p^+ and n^+ electrodes of the detector when the absolute value of bias voltage is larger than 8 volts, which ensures the carrier saturation drift velocity condition, and therefore a fast charge collection time of about 100 ps.

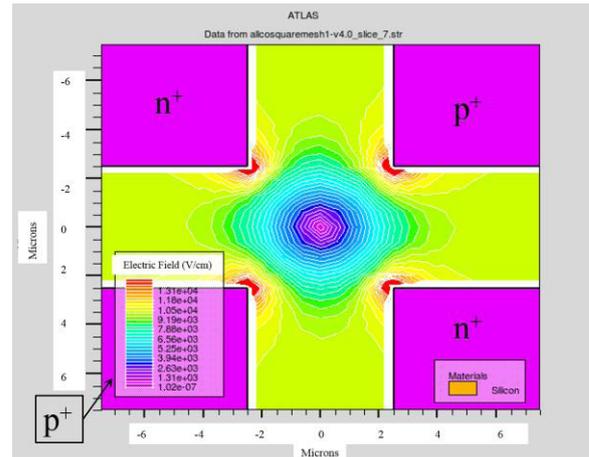


Figure 5. Electric field profile of a detector with a column spacing of 5 μm . The bias voltage is -4volts. Maximum electric field shown is 1.5×10^4 V/cm.

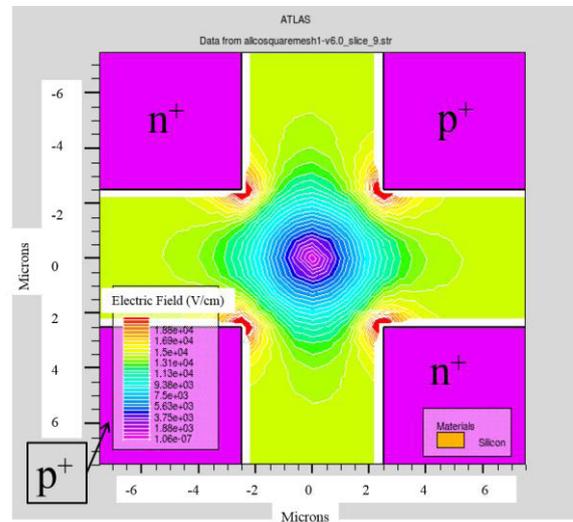


Figure 6. Electric field profile of a detector with a column spacing of 5 μm . The bias voltage is -6volts. Maximum electric field shown is 2×10^4 V/cm.

However, as we can see from Figure. 5-8, the electric field in the central region of the detector is very low even at high bias voltages. This is due to the symmetry structure of this type of 3D detector (all column electrode detectors). Usually, a slow region is defined as the region near the cell center where there is an electric potential saddle point with zero electric field. Due to the low field, the carrier drift velocity will be low as well

If we use an electric field value of $\leq 5 \times 10^3$ V/cm as

the low electric field limit that defines the border with the ultra-fast charge collection region, then we can estimate the percentage of the region with low electric field (the "slow region") as the following:

for $L_p = 5\mu\text{m}$, the proportion of the "slow region" is: 9.07% $((1.9 \times 1.9 \times 3.1416)/(5 \times 5 + 4 \times 5 \times 5))$, and for $L_p = 10\mu\text{m}$, the proportion of the "slow region" is: 9.42% $((3 \times 3 \times 3.1416)/(10 \times 10 + 4 \times 10 \times 5))$.

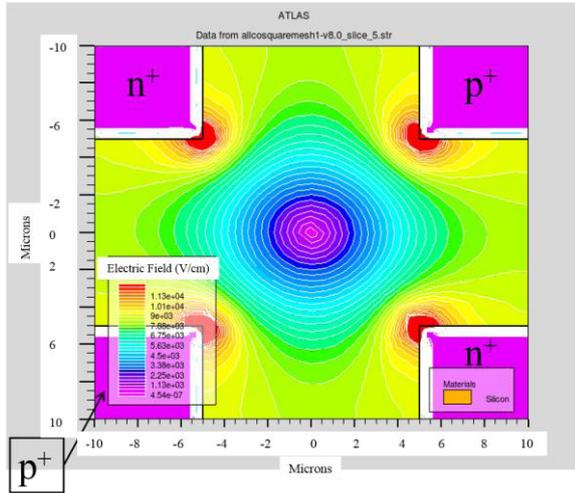


Figure 7. Electric field profile of a detector with a column spacing of 10 μm . The bias voltage is -8 volts. Maximum electric field shown is 1.2×10^4 V/cm.

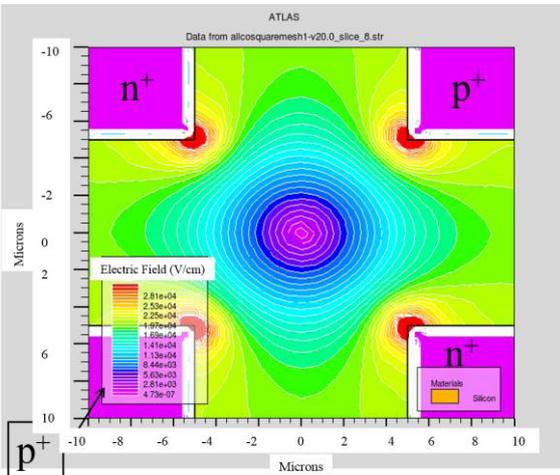


Figure 8. Electric field profile of a detector with a column spacing of 10 μm . The bias voltage is -20volts. Maximum electric field shown is 2×10^4 V/cm.

In both cases, they are below 10%. Meanwhile, since the electrode spacing is extremely small, in the order of the size of electrode columns, the relative dead region (non-sensitive region) will be large. In fact, for $L_p = 5\mu\text{m}$, the dead region is 25% (in a unit cell, the dead column area is $4 \times 1/2 \times 25 \mu\text{m}^2 = 25 \mu\text{m}^2$, and the sensitive area is $(4 \times 1/2 + 1) \times 25 \mu\text{m}^2 = 75 \mu\text{m}^2$), and for $L_p = 10\mu\text{m}$, it is 12.5%. Therefore there is a trade-off between the ultra-fast and large relative dead-space.

The full depletion voltage can be estimated as:

$$V_{fd} = \frac{qN_D L_p^2}{2\epsilon_0 \epsilon} \quad (4)$$

Here N_D is the detector bulk doping concentration. The doping of the silicon bulk is $1 \times 10^{12} \text{ cm}^{-3}$. When the column spacing is 5 μm or 10 μm , the depletion voltage is very small.

4 Breakdown Consideration

Even though the absolute values of applied bias voltages are small, (≤ 10 volts), due to the nature of small device with very small electrode spacing, there could be local high field regions where intrinsic breakdown field for Si ($\sim 300 \text{ KV/cm}$) may be reached. Such high fields can exist especially near the corners of p^+ columns, just under oxide layers. We cut the profile just under the oxide layer (Z-direction, at $z=1\mu\text{m}$) as shown in Figure.9 ($L_p = 5\mu\text{m}$, the bias voltage is -8 volts) and Figure.10 ($L_p = 10\mu\text{m}$, the bias voltage is -9 volts). From the cutline between two p^+ columns, presented in Figure.11 and Figure.12, we can read that the largest value of the electric field is about $9 \times 10^4 \text{ V/cm}$ and $6.7 \times 10^4 \text{ V/cm}$ respectively, which are all smaller than $3 \times 10^5 \text{ V/cm}$, the intrinsic breakdown field in Silicon. This means that the detector does not reach breakdown even when the saturation velocity is reached at biases voltage conditions as suggested in this work.

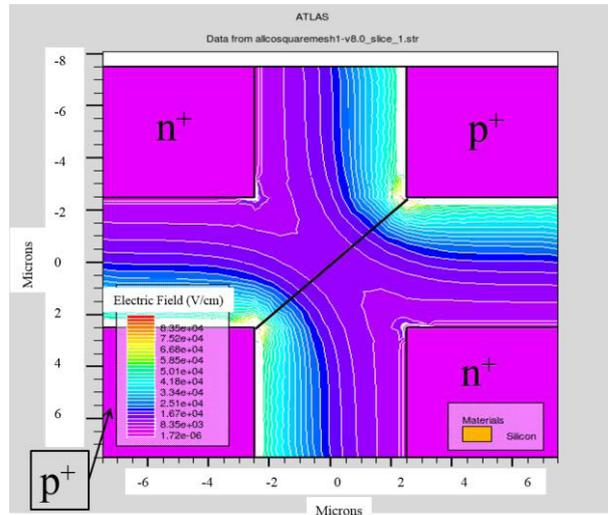


Figure 9. Electric field profile of a detector with a column spacing of 5 μm . The bias voltage is -8 volts.

5 Summary

From calculations and full 3D simulations, we conclude that the ultra-fast charge collection time ($\leq 100 \text{ ps}$) can be obtained at a bias voltage of only a few volts (≤ 10 volts) for small 3D detectors with electrode spacing less than or equal to 10 μm . As we simulated in this study, we can get a minimum carrier drift time of about 50 ps in most part of the detector when L_p is 5 μm , and a minimum carrier drift time of about 100 ps in most part of the detector when L_p is 10 μm . The full depletion voltages for these types of detectors are less than 1 volt.

However, because of the symmetry structure of the all column electrode type 3D detectors, a low electric field region exists in the center of the detector regardless of the detector bias voltage. This is the shortcoming of this type of 3D detector. We are working on a new structure to solve this problem [2-5]. Also, we investigated the possible breakdown situation in this type of detectors, and found that at the minimum voltages to reach carrier drift velocity saturation, the highest electric field in the detector is much below the value of the Si intrinsic breakdown field.

We note here that those type of 3D detectors are intrinsically rad-hard due to their very small electrode spacing, and we will study this further.

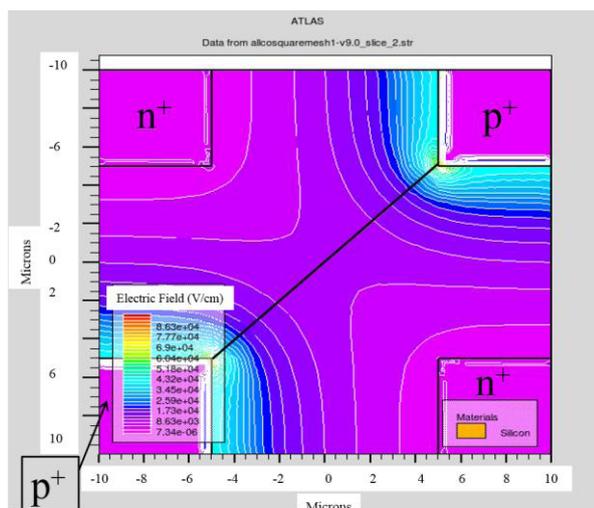


Figure 10. Electric field profile of a detector with a column spacing of 10 μm . The bias voltage is -9 volts.

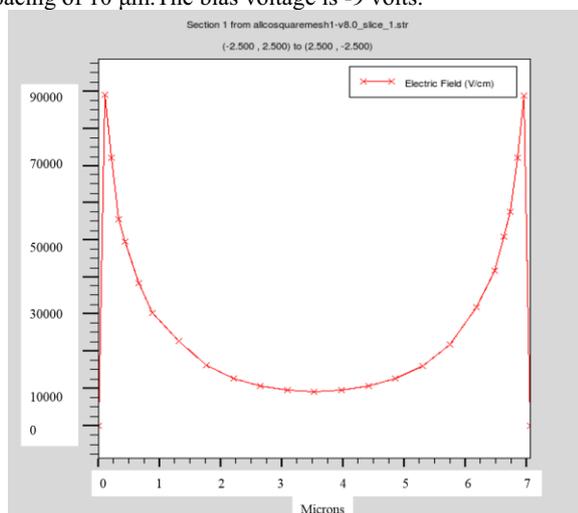


Figure 11. Electric field outline of a detector with a column spacing of 5 μm . The bias voltage is -8 volts.

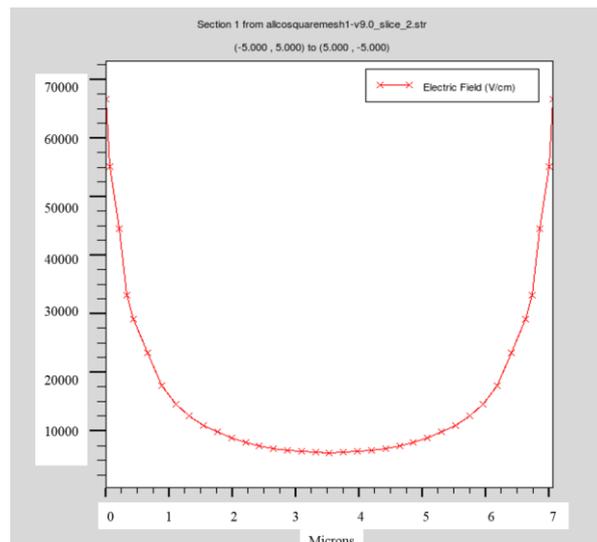


Figure 12. Electric field outline of a detector with a column spacing of 10 μm . The bias voltage is -9 volts.

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