The Influence of Gate Scaling to Electrical Characteristics on n-MOS FinFET

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Abstract. This paper investigates effects from gate scaling in Tri-gate FinFET structure by simulation method, to avoid problems and improve a structure to be good prototype. The experiments used GTS framework for simulation. Start from 20 nm device, then scaling to 22 nm 28 nm and 32 nm. Therefrom Minimos-NT function has used for biasing to giving two electrical characteristics as the drain current saturation and the threshold voltage. From these consequences can offer the subthreshold swing and the drain-induced barrier lowering by calculation. The results found that threshold voltage inversely proportional to saturated drain current, the subthreshold swing and the drain-induced barrier lowering. The short channel effect has affected to 20 nm model by highest DIBL. Therefore should be adjust the gate length and the oxide thickness properly to improve this effect.

1 Introduction

The introduced of Tri-gate transistor technology by Intel corporation in 2nd quarterly of 2011. Intel brought the new technology to giving good performance for them devices. 3-D transistor as known as FinFET. This is a choice to make new computer architecture. In 2011 M. Zakir Hossain and his researcher team shown electrical characteristics of SOI tri-gate FinFET. The result of this paper explain about basic characteristics such as the current and voltage characteristics (I-V), the threshold voltage, the electron mobility and field mobility [1]. In 2012 they proposed about the drain-induced barrier lowering (DIBL) and short channel effect (SCE). Influence of DIBL and SCE is coming together. DIBL make a drain to gate electron barrier lower. In a same way I-V and threshold voltage will strange from theory, and downward a subthreshold characteristics. It make device cannot change to cut-off stage at low voltage [2]. This concept make author interested in effects from scaling a device to solve problems for improved a structure of FinFET prototype and fabrication in the future.

2 Theory

2.1 Saturation Drain Current ($I_{ds,Sat}$)

While the drain current has no longer affected by the drain voltage, and where the FinFET acts more like a current source, has called the current saturation. This current value can be solve by [3]:

$$I_{ds} = \mu C_{ox} \frac{W_g}{L_g} \left(\frac{v_{gs} - v_{th}}{2m} \right)^2 \quad (1)$$

W_g, gate width (nm) L_g, gate length (nm) C_{ox}, Gate Oxide capacitance (F/nm)

2.2 Threshold Voltage (V_{th})

The minimum gate-to-source voltage differential that was needs to create a conducting path between the source and drain. This is the most significant characteristic that provide the value of power that used to switch the FinFET from off stage to on stage and show the switching performance of devices. The threshold voltage can giving from [4]:

$$V_{th} = \Phi + \frac{kT}{q} \ln \left(\frac{2C_{ox} kT}{q^w n_i t_{si}} \right) + \frac{h^2 \pi^2}{2m W_{si}^2} \quad (2)$$

n_i, Electron and Hole Concentration without Doping (cm^{-3}) t_{si}, Silicon Thickness (nm) h, Channel Height (nm) w_{si}, Silicon width (nm) η, Carrier Concentration (cm^{-3}).

2.3 Subthreshold Swing (SS)

The subthreshold swing is logarithm of drain current relationship of drain current and gate voltage that

determine the voltage per decade. The solution to find a subthreshold swing, can calculate with equation (3) [5] by methods in Figure 1.

$$SS = V_{gs2} - V_{gs1} \quad (3)$$

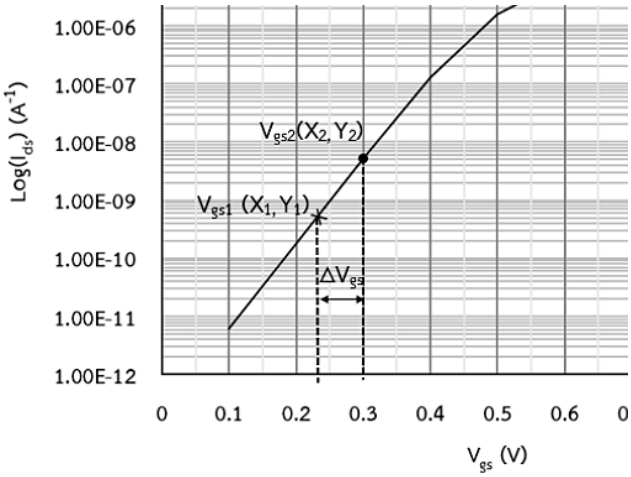


Figure 1. Relationship between the drain current and the gate-source voltage

2.4 Drain-Induced barrier lowering (DIBL)

The reduction of threshold voltage at higher drain voltages by the lowering of potential barrier on drain that affect to gate and Solve by [6]

$$DIBL = \frac{V_{th}^{Low} - V_{th}}{V_{dd}^{Low} - V_{dd}} \quad (4)$$

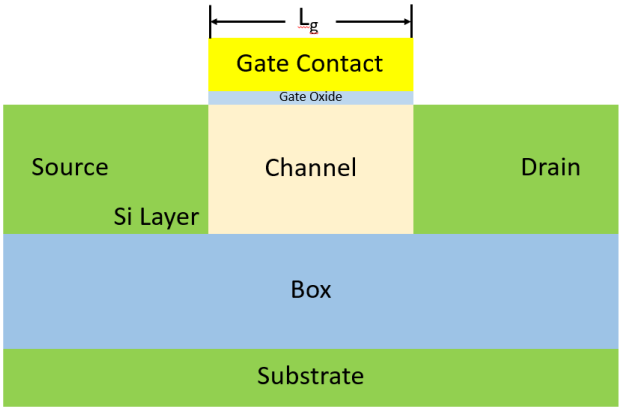
3 Experimental

This paper separated to two experiments part consist of the FinFET structure and the relationship between the electrical characteristics with the gate length. The first part, create a device structure on GTS framework [7] from 20 nm gate length and then increase L_g to 22 nm, 28 nm, and 32 nm 10 nm silicon layer width and 25 nm silicon thickness with 1 nm gate oxide thickness on the top of 70 nm p-type substrate with buried oxide (BOX). In second part, Minimos-NT has use for biasing to obtain the electrical characteristics by determined the drain voltage at 1 volt and sweep the gate voltage from 0 to 1 volt (0.1 volt per steps) for harvest the threshold voltage. Collect the I-V characteristics by fixed the drain voltage at 1 volt and vary the gate voltage from 0 to 1 volt (0.1 volt per steps) and calculate the saturation regions of drain current. After collected V_{th} and I-V, calculate the subtheshold slop from $\log(I_{ds})/V_{gs}$ and DIBL from V_{th} finally compare with gate length to giving the results of gate scaling effect.

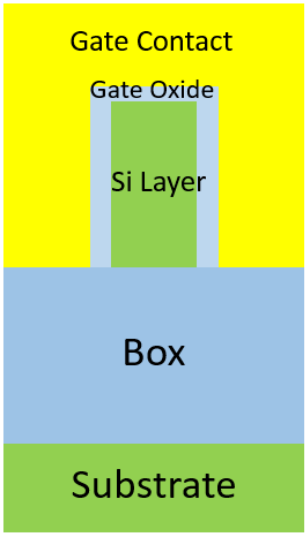
4 Result and Discussion

4.1 FinFET Structure

From the first experiment part, created a FinFET structure that consist of the substrate, BOX, the silicon layer, channel, gate oxide and gate contact shown in Figure 2. (a) Side view of device with the gate length. (b) Cross section shown a fin width under oxide and contact, all of those are on buried oxide and the substrate. In this structure, determined the dopant concentration on channel at 1.5×10^{15} cm^{-3} and 3×10^{20} cm^{-3} on drain-source with poly-silicon gate contact therefore this part will provide four structures with difference of the gate length.



(a)



(b)

Figure 2. FinFET Structure (a) Side view (b) Cross Section

4.2 Characteristics with gate length relationship

The electrical characteristics of devices is the important point to determine a performance. From second part of experiment obtain the drain current saturation, the threshold voltage for calculate the subthreshold swing and the drain induced barrier lowering, to compare-between characteristics and enlargement of gate length.

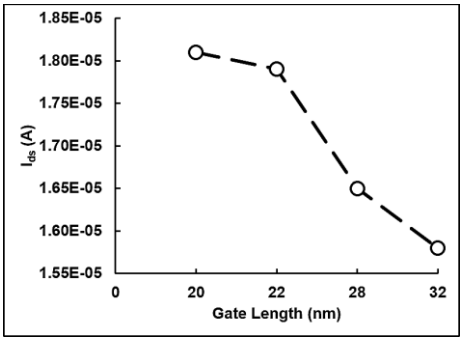


Figure 3. Drain current saturation with gate length

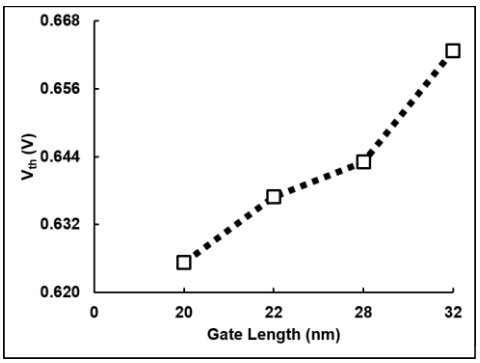


Figure 4. Threshold voltage with gate length

An enlargement of gate length determined a saturation current in Figure 3. The deportment of I_{ds} was lowering with increase of L_g. Due to adding of electron concentration in channel that affect to them mobility. This effect bring I_{ds} downward about 0.1 µA per increasing of L_g. It was giving I_{ds} on 20 nm ate length at 18.10 µA, 22 nm at 17.90 µA, 28 nm at 16.50 µA and 32 nm at 15.80 µA. Therefore $I_{ds\ (Sat)}$ behaviour on device with 20 nm L_g is better. In Figure 4, the threshold voltage has increased with L_g but after biased I_{ds} / V_{gs} giving amiss result of 20 nm. It was coming with a little SCE because in this experiment vary only L_g. The threshold voltage of 20 nm gate length about 0.625 volt, 22nm at 0.636 volt, 28 nm at 0.643 and 32 nm gate length has 0.662 volt thus SCE affect to this characteristics directly while gate length was increased. Normally, V_{th} will increasing with L_g since the gate length has increased and require more energy to turn device stage to turn-on.

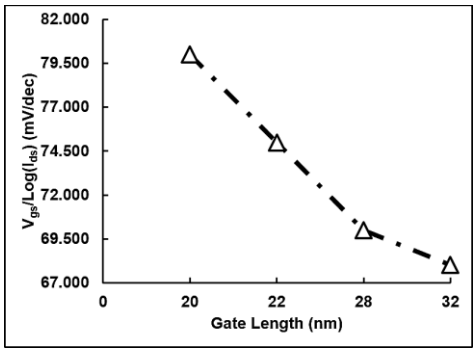


Figure 5. Subthreshold Swing with gate length

In Figure 5 shown the subthreshold swing has decreased by the gate length increasing, as more drain current passing in shorter L_g. From logarithm square root of drain current and gate-source voltage provide the SS on 20 nm L_g = 80 mV/dec, 22nm = 75 mV/dec, 28 mV = 70 and 32 nm gate length at 68 mV/dec.

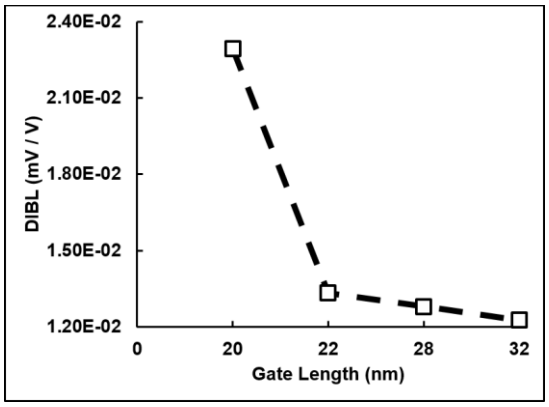


Figure 6. DIBL with gate length

The subthreshold swing is important attribute to obtain DIBL with gate length that shown in Figure 6. Influence of DIBL was directly to SS from lowering of barrier between channels and drain junction that affect to threshold voltage. DIBL on 20 nm gate length was about 23 mV/V, 22 nm at 13.30 mV/V, 28nm at 12.80 mV/V and 32 nm L_g approximate about 12.30 mV/V. The DIBL giving to known a problem from SCE. If it was high, this device will be out of characteristics.

Table 1. Electrical characteristics of FinFET

Gate Length (nm)	$I_{ds(sat)}$ (µA)	V_{th}(V) (V_{dd} = 1 V)	SS (mV/dec)	DIBL (mV/V)
20	18.10	0.62	80.00	23.00
22	17.90	0.63	75.00	13.30
28	16.50	0.64	70.00	12.80
32	15.80	0.66	68.00	12.30

From Table 1, Increasing of gate length will bring the threshold voltage up but the drain current, the subthreshold swing and DIBL are inversely proportional. The highest DIBL of 20 nm giving a least V_{th} that affected by short channel effect not from decreasing of gate length.

5 Summary

Investigate into FinFET structure simulation is best way to understand operating of device. Many of problems has found from this experiment. In this article provides experiments to bring up effects from designed device structure, which are two effects as the short channel effect and the drain-induced barrier lowering. From the result found relationship between the drain current saturation, the threshold voltage, the subthreshold swing and the drain-induced barrier lowering. Increasing of gate length directly with V_{th} but reverse with $I_{ds,sat}$, SS and

DIBL. The short channel effect has found in 20nm model therefore an adjustment of gate length will reach electrical characteristics suitability.

Acknowledgement

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