Additive effects under the series of EOS in space application VLSI circuits

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Abstract. One of the problems of space technology is the spacecraft on orbit charging effect. Series of EOS (electrical overstress) are caused by internal charging affect VLSI (very large-scale integrated) circuits, which may lead to its damage. The results of the EOS series with energy below the threshold of failure for modern submicron VLSI circuits design are presented. The obtained results confirm the possibility of accumulation of the effects of damage from exposure of EOS series in modern VLSI circuits and allow you to get the dependence describing the additive nature of damage the VLSI circuits during exposure to subthreshold EOS. The obtained dependence agrees well with the Arrhenius equation, which indicates the thermal nature of the damage under the series of subthreshold energy EOS. The method of the VLSI circuits testing is proposed to determine the level of the VLSI circuits EOS hardness to the effects of multiple different pulsing voltages.

1 Introduction

The space industry has currently faced the problem of the spacecraft lifetime. One reason for the decrease in lifetime of the spacecraft is the charging effect [1].

The charging effect of the spacecraft is caused by exposure to a flow of charged particles near-Earth plasma, the solar wind, galactic radiation and light. Different parts of the spacecraft accumulate charge unevenly as a result of its non-uniform irradiation and the use of different materials in the structure. Over time, it has formed between the parts defined potential difference, and electrostatic forces act. When the electric field strength exceeds the critical (for near-Earth space plasma $E_{max} \sim 10^7$ *V/m*) electrical discharge occurs between the parts of the spacecraft, which can lead to malfunctions and damages of sensitive electronics of the spacecraft.

The internal charging effect is caused by the accumulation of charge by particles penetrating within the spacecraft body. Charged particle energy over 100 keV penetrate the spacecraft casing and is absorbed by dielectrics and ungrounded conductors located in a part of the sensitive electronics (Figure 1). Despite the relatively small flow of high-energy charged particles and small amplitude of discharge pulse internal charging effect can have a significant impact on the operation of the spacecraft [1]. The reason is the direct impact of EOS on sensitive components [2].

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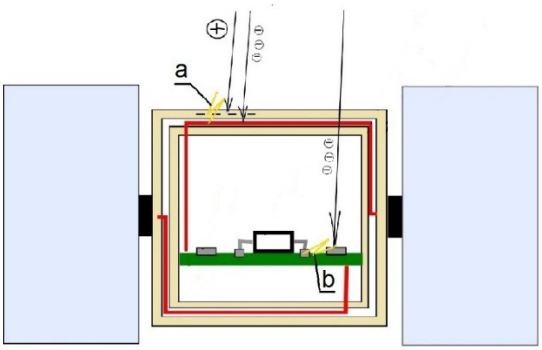

Fig. 1. EOS in outer shell of the spacecraft caused by the external charging effect (a) and EOS between terminal of VLSI circuit and ungrounded conductor caused by the internal charging effect.

Electrical discharges caused by internal charging effect leads to the appearance of the voltage pulses at terminals of electrical components. Amplitude of the voltage pulses may be up to ten and hundreds volts [2].

During the entire period of operation of the spacecraft many internal electrical discharges occur. Over 10 years of operation, their number can reach about 10^4 [3]. Thus, the series of electrical discharges caused by the internal charge effect will affect terminal of a single VLSI. Under the influence of the additive effect of damage accumulation in VLSI circuits, failure may occur when the EOS energy is below the threshold of failure [4].

The article presents the results of an experiment on the effects of a series of subthreshold energy pulse voltage CMOS IC CD4007. This data confirms the presence of additive effects in CMOS circuits [5].

For a more detailed research of this effect, the impact of EOS series on the behaviour of two types of modern controllers was studied.

2 Materials and methods

The specialized pulse voltage generator (EMI-0501) was used to estimate the EOS behavior. The EOS pulses were applied between the ground and appropriate pin. The impact of EOS was repeated until the failure of VLSI circuit was recorded.

Test procedure and generator parameters are described in [6].The LVSI circuit under test was connected through the buffer unit to a storage oscilloscope and a functional control module.

3 Results

Dependence $N(U_{EOS})$ was obtained for each type of microcontrollers, where N - number of voltage pulses of amplitude effects U_{EOS} until sample failure. These dependences are shown in Figure 2.

The following function (1) provides the best fit to obtained data for all types of microcontrollers.

$$N(U_{EOS}) = \exp(b(\frac{1}{{U_{EOS}}^2} - \frac{1}{{U_O}^2})) \quad (1)$$

Where U_O - amplitude threshold of the failure for this type of LVSI circuit, b - parameter of approximation, depending on the product type.

Linear approximation (2) in semi-logarithmic scale on the x axis was obtained based on the results (Figure 3).

$$N(x = b(\frac{1}{U_{EOS}{}^2} - \frac{1}{U_O{}^2}) \quad (2)$$

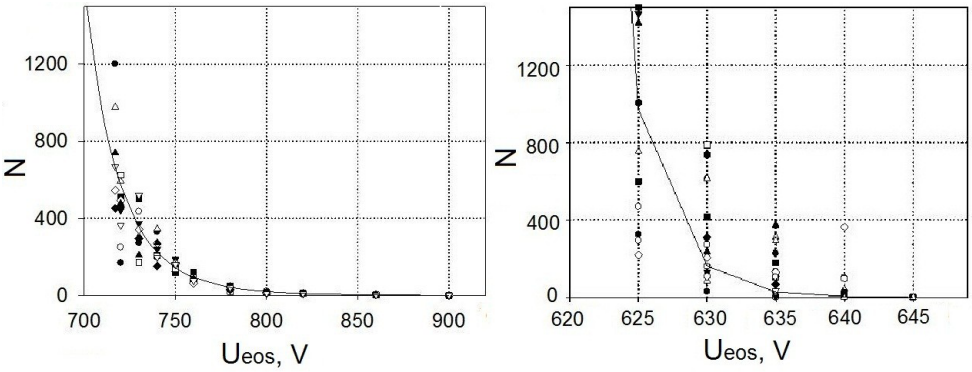

Fig. 2. Dependences $N\ (U_{EOS})$ for MC ATtiny13A (left) and MC PIC24F16KA101-I / MQ (right).

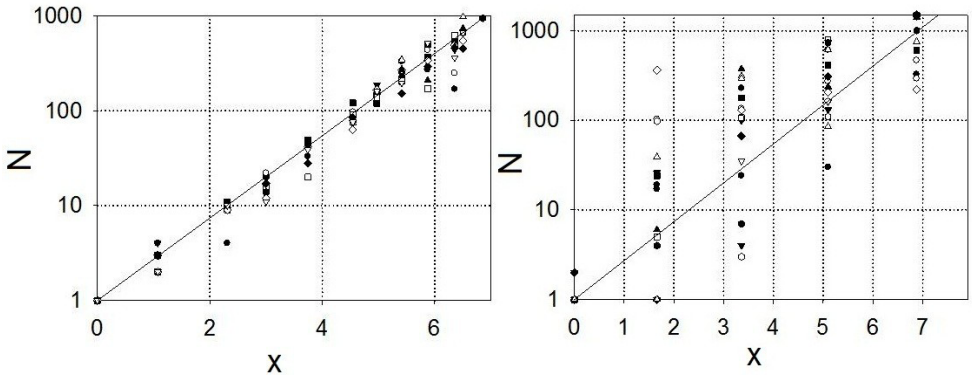

Fig. 3. Linear approximation $N(x)$ for MC ATtiny13A (left) and MC PIC24F16KA101-I / MQ (right).

4 Discussion

The dependence shown in Figure 2 shows that for different types of VLSI circuits investigated voltage range (for which the number of the voltage pulse impact was relatively small $N(U_{EOS}) < 1000$) varied considerably. From this, it follows that for VLSI circuits experiencing during operation a large number of EOS effects, critical voltage amplitude U_{CR} may be substantially below the threshold of failure when exposed to a single EOS pulse.

Therefore, the design of electronics is necessary to consider EOS caused by internal charging, and their impact on the performance of the element base, especially in the long term of operation.

The results of approximation (1) comply well with the Arrhenius equation. (3)

$$\nu^{-1} = \exp(\frac{E_a}{kT}) \quad (3)$$

v^{-1} - the inverse of the speed energy-dependent processes in the semiconductor and corresponds to the number of impacts N and the kT - corresponds to the stress caused by the EOS pulses (U_{EOS}^2 determines the power that is in the chip element). The difference in the reverse voltages of squares obtained dependence is related to the ratio of the electrical stresses at the points U_O and U_{EOS}.

5 Conclusions

From experimental results it follows that it is desirable to conduct tests on the sensitivity of the components that make up the spacecraft electronics, to the effects of EOS series.

For dependence $N(U_{EOS})$ there is no need to destroy a large number of chips. It is sufficient to determine the amplitude threshold failure U_O and obtain the value $N(U_{EOS})$ at one point. This makes it possible to carry out tests on the IC (integrated circuits) sensitivity to EOS series of subthreshold energy at low cost.

The obtained dependence complies well with the Arrhenius equation, which indicates the thermal nature of the damage when exposed to series of subthreshold EOS.

References

1. D.L. Mulville, *NASA Technical Handbook,* **4002** (1999)
2. A.R. Frederickson, *Spacecraft Charging Technology, Proceedings of the Seventh International Conference held 23-27 April*, 417 (2001)
3. W. Kim, I. Jun, M. Kokorowski, IEEE Trans. on Nucl. Sci. **57**, 3143 (2010)
4. M. Gorlov, A. Stroganov, A. Adamian, ChipNews **1**, 34 (2001)
5. P. Skorobogatov, K. Epifantsev, *Conf. Scientific session of the MEPhI, theses*, 108 (2013)
6. P.K. Skorobogatov, *Proceedings 4th European Conference on Radiations and Its Effects on Components and Systems (RADECS 97)*, 174 (1997)