Synchronization Time Division Multiplexing Bus Communication Method Using Serial Communication Interface

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Abstract. It provided a synchronization time division multiplexing bus communication method using serial communication interface, in which input and output data lines of a host and several slaves being connected with the bus. Then the detailed communication mode was stated. The method could be applied in all MCU, meanwhile meets the requirements of high speed for the real time performance, and solves the problem of bus communication between internal modules of a device and realizes controllable communication real time performance, reduced hardware circuit complexity as well as enhanced universality and reliability.

1 Field of invention

At present, bus is commonly utilized as communication channels between the master board and the input or output board in automatic devices. On the input or output board MCU is provided for processing a variety of input or output signals, which communicates with the MCU on the master board. Consequently the timeliness and stability of automatic devices is dependent on architecture of the internal bus. However, normal serial or parallel communication manner could not meet requirements of real time communication under strong interference [1,2]. As a result, the manufacturers proceed to develop respective bus for their own devices so as to achieve the requirements of real time communication under strong interference. However, due to the fact that there is a wide variety of internal bus, such as parallel bus and serial bus, bus formed by FPGA and formed by CPLD, as well as formed by MCU of other types, bus with SPI interface and with SCI interface, as well as with CAN interface or other types of interface, it's very difficult to develop a bus with desirable simple architecture applicable to the communication between the master board and the input or output board using short and fixed length communication messages, thus making the requirements for real time communication hard to be achieved [3,4].

2 Summary of invention

The object of the present invention is to overcome above disadvantages in prior art. There is provided a synchronization time division multiplexing bus communication method, which utilizes just two physical connection lines to implement differential connection with high reliability and meet the requirements of high speed for real time communication on the basis of most ordinary MCUs, thereby solving the problem in bus communication between internal modules of a device and enabling for controllable communication real time performance, reduced hardware circuit complexity as well as enhanced universality and reliability [5,6].

The above objects of the present invention are achieved by the following technical solutions:

A synchronization time division multiplexing bus communication method using serial communication interface, including a host and plural slaves, the host and slaves all comprising SCI (Serial Communication Interface) and timer provided micro control unit (MCU), the input and output data lines of the host and slaves all being connected with the bus, characterized in that, the bus communication method is as follows: each time when the host sends a down-link data message required by respective slaves, the slaves receive the data via the SCI and proceed to send up-link data messages after waiting for a time interval, and each time when a previous slave completes to send the up-link data message, the next slave begins to send the up-link data message after waiting for an identical time interval, and so on, until the bus communication method is accomplished.

Preferably, the slaves send the up-link data messages in such a manner that after a slave receives data, determine whether the data is host data or not; if the data is not host data, the slave doesn't process the data and continue to receive data; and if the data is host data, the slave initiates the timer and implements data validation to the received host data; in

the case of validation failure the slave turns off the timer and continues to receive data, and in the case of validation success, the slave proceeds to process data; when the timer interruption occurs, the slave sends data message via the SCI.

In order to enhance communication reliability and reduce bit error rate, in terms of bus physical architecture, the bus is converted into differential lines by a single-ended differential signal conversion chip, and the host and slaves are connected to the bus via the differential lines.

Preferably, the time interval mentioned above is a period of an Idle.

Preferably, the bus utilizes half-duplex communication mode.

By the above method, the bus physical architecture of the present invention could be simplified, in which real time bus communication with high reliability could be realized only using two differential lines, and the requirements of high speed for the real time performance could also be achieved. In the case of low external interference real time bus communication could be realized using even only one signal lines. The bus could be implemented using any kind of MCU provided with SCI and timer, therefore the demand for MCU hardware is low. For different slaves, respective baud rate and waiting time could be chosen according to actual situation so as to meet real time requirements. As synchronization time division multiplexing method is employed, the host could fill data memory according to the time interval, and the procedure for processing bus data of the slaves could be simplified. The message sent by the host could be used as beat of message transmission of the slaves. Each time when the host sends a message, time setting could be made to the slaves, thus ensuring the accuracy of transmission beat of the slaves. Variable period could be selected based on task amount of the host to eliminate loss of synchronism of the slaves. The present invention solves the problem of bus communication between internal modules of a device and realizes controllable communication real time performance, reduced hardware circuit complexity as well as enhanced universality and reliability.

3 Brief describe of the drawings

Figures and tables, as originals of good quality and well contrasted, are to be in their final form, ready for reproduction, pasted in the appropriate place in the text. Try to ensure that the size of the text in your figures is approximately the same size as the main text (10 point). Try to ensure that lines are no thinner than 0.25 point.

The present invention will be further described in detail below in connection with embodiment and accompanying drawings,

Figure 1 is a schematic diagram showing system configuration in an embodiment of the present invention

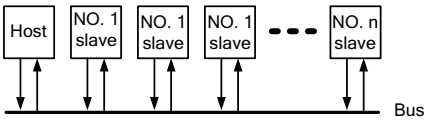

Fig. 1. System diagram.

Figure 2 is a schematic diagram showing format of a message frame with address bit in the embodiment of the present invention [7];

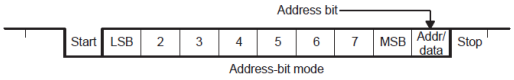

Fig. 2. The diagram of communication format.

Figure 3 is a schematic diagram showing communication procedure in the embodiment of the present invention;

Fig. 3. The diagram of communication process.

Figure 4 is a flow chart showing a salve sending uplink data message in the embodiment of the present invention.

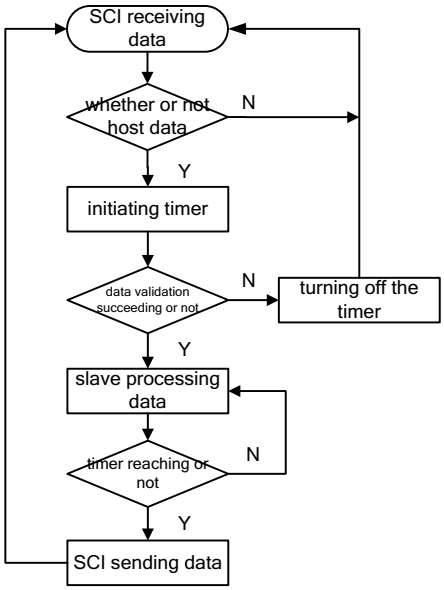

Fig. 4. The diagram of software process.

4 Describe of preferred embodiment

These and other aspects, features and advantages of which the invention is capable of will be apparent from the following description of embodiment of the present invention.

Referring to Figure1, there is provided synchronization time division multiplexing bus communication method using serial communication interface to solve the problem of bus communication between internal modules of a device. The bus utilizes half-duplex communication mode, which could realize real time bus communication with high reliability and meet the requirements of high speed for the real time performance. In the embodiment of the present invention, the input and output data lines of the host and multiple slaves are all connected with the bus. At any time only one equipment occupies bus resource to send data, and other equipment receives data. In order to enhance communication reliability and reduce bit error rate, in terms of bus physical architecture, the bus is converted into differential lines by a single-ended differential signal conversion chip, i.e. differential lines are utilized to send and receive data, and the host and slaves are connected to the bus via the differential lines.

Figure 2 is a schematic diagram showing frame format of a message with address bits in the embodiment of the present invention. As shown in Figure 2, there is a start bit, a data bit, an address bit and a stop bit. A message frame with address bit is employed for communication in the embodiment, which is accomplished as follows:

The communication loop is divided into up-link message and down-link message, wherein the down-link message has an address bit of "1" and is sent from the host to the slaves. In the manner of "one host and multiple slaves" and "the slaves receive what the host sends", the slaves pick up desired information respectively from the message received. The rate of the down-link message is treated as operation beat of the slaves.

The up-link message has an address bit of "0" and is sent from the slaves to the host in a time division multiplexing manner. When a slave receives a message with address bit of "1", it sends up-link data after a certain delay time period according to its own address number, thereby achieving multiplexing. When a slave receives a message with address bit of "0", it doesn't handle it.

In the embodiment the symbol "T_{host}" represents the time period of sending down-link message by the host, and the symbol "T_{slave}" represents the time period of sending up-link message by each slave, and the symbol "$Idle$" represents the waiting time between two times of sending.

Referring to Figure3, A synchronization time division multiplexing bus communication method using serial communication interface is provided in the embodiment, in which the host sends a down-link data message, the NO 1 slave receives the data via the serial communication interface, i.e. SCI and proceeds to send up-link data messages after waiting for a time interval equal to $Idle$; and after waiting for a time interval equal to $Idle$ again, the NO 2 slave proceeds to send up-link data messages, and so on. The NO N slave proceeds to send up-link data messages after waiting for a time interval equal to $Idle$, and then the host sends a down-link data message once more after waiting for a time interval equal to $Idle$, thereby the data communication being completed.

The slave opens the SCI and proceeds to receive the data message, then determines whether the address bit indicates host data or not. In the case of other slave data, it will not be handled. In the case of host data, the slave initiates the

timer (the timing length is dependent on $Idle$, T_{slave} and N). Then the slave implements data validation to the received host data. In the case of validation failure the slave turns off the timer and continues to receive data, and in the case of validation success, the slave proceeds to process data. When the timer interruption occurs, the slave sends data message via the SCI.

The time for message sending is calculated as follows:

the sending time t_n of the Nth slave:

$$t_n = Idle + (Idle + T_{slave}) \cdot (n-1) \tag{1}$$

in which n is address number from 1 to N;

And one communication cycle T:

$$T = T_{host} + Idle + (Idle + T_{slave}) \cdot n \tag{2}$$

in which n is address number from 1 to N.

The one communication cycle T and the maximum number of slaves in system could be determined according to actual requirements of the system, and appropriate baud rate and waiting time could be chosen to accomplish data communication within predetermined period of time. For example, provided the communication cycle of the system is 500us, the maximum number of slaves is 10, the baud rate is set as 3.75mbps, and the down-link message of the host has 16 bytes while the up-link message of the slaves has 10 bytes, then the waiting time,

$$Idle = [500 - (16 \cdot 11/3.75) - 10 \cdot (10 \cdot 11/3.75)]/(10+1) \approx 14.5us \tag{3}$$

By setting above waiting time for the slaves, real time communication with cycle of 500us could be achieved.

In conclusion, the bus physical architecture of the present invention could be simplified, in which real time bus communication with high reliability could be realized only using two differential lines. In the case of low external interference real time bus communication could be realized 1using even only one signal lines. The bus could be implemented using any kind of MCU provided with SCI and timer, therefore the demand for MCU hardware is low. For different slaves, respective baud rate and waiting time could be chosen according to actual situation so as to meet real time requirements. As synchronization time division multiplexing method is employed, the host could fill data memory according to the time interval, and the procedure for processing bus data of the slaves could be simplified. The message sent by the host could be used as beat of message transmission of the slaves. Each time when the host sends a message, time setting could be made to the slaves, thus ensuring the accuracy of transmission beat of the slaves. Variable period could be selected based on task amount of the host to eliminate loss of synchronism of the slaves.

The internal bus of the present invention only uses two differential lines to implement differential connection with high reliability on the basis of most common MCU, meanwhile meets the requirements of high speed for the real time performance.

5 What is claimed is

1). The synchronization time division multiplexing bus communication method using serial communication interface, including a host and plural slaves, the host and slaves all comprising Serial Communication Interface and timer provided micro control unit, the input and output data lines of the host and slaves all being connected with the bus, characterized in that, the bus communication method is as follows: each time when the host sends a down-link data message required by respective slaves, the slaves receive the data via the SCI and proceed to send up-link data messages after waiting for a time interval, and each time when a previous slave completes to send the up-link data message, the next slave begins to send the up-link data message after waiting for an identical time interval, and so on, until the bus communication method is accomplished.

2). The synchronization time division multiplexing bus communication method using serial communication interface according to claim 1, characterized in that, the slaves send the up-link data messages in such a manner that after a slave receives data, determine whether the data is host data or not; if the data is not host data, the slave doesn't process the data and continue to receive data;

and if the data is host data, the slave initiates the timer and implements data validation to the received host data; in the case of validation failure the slave turns off the timer and continues to receive data, and in the case of validation success, the slave proceeds to process data; when the timer reaches, the slave sends data message via the SCI.

3). The synchronization time division multiplexing bus communication method using serial communication interface according to claims 1 or 2, characterized in that, in terms of bus physical architecture, the bus is converted into differential lines by a single-ended differential signal conversion chip, and the host and slaves are connected to the bus via the differential lines.

4). The synchronization time division multiplexing bus communication method using serial communication interface according to claims 1 or 2, characterized in that, the time interval mentioned above is a period of an Idle.

5). The synchronization time division multiplexing bus communication method using serial communication interface according to claims 1 or 2, characterized in that, the bus utilizes half-duplex communication mode.

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