Comparison Between Different Ways in Making Silicon Dioxide Layer on Silicon Wafers

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Abstract. The most important raw material for power device is epitaxial wafers, which is made from heavily doped polishing silicon wafers. In order to prevent dopant doped into silicon while pulling ingots spread into the epitaxial atmosphere and finally into the Epitaxial layer, while polishing wafers are produced, silicon dioxide layer will be added on the back surface of silicon wafers. There are two ways mainly used to make this silicon dioxide layer, one is named High Temperature Oxide (HTO), and the other is named Atmosphere Pressure Chemical Vapor Deposition (APCVD). The process parameter such as temperature, time and pressure are quite different from each other, also the character of the silicon dioxide layer and the effect that silicon dioxide layer have on the wafers are different from each other. In this article we will compare the difference between the two silicon dioxide layers and the ways in making silicon dioxide layers.

1 INTRODUCTION

Power Semiconductor is also known as Power Electronic Device, including Discrete Device and Integrated Circuit, mainly used in transforming and controlling current, voltage, frequency and so on in order to achieve the function as rectification, inversion, chopping, amplifier etc. Because these kinds of devices can endure high voltage large current, they play more and more important roles in nowadays society[1]. Together with the improvement of Power Semiconductor the requirement of the main raw material for power semiconductor is becoming more and more strict, also the requirements of polishing wafers is becoming more and more strict.

Epitaxial process is a high temperature process. During this process substrate character will have a lot effect on epitaxial layer, such as defects and WARP data. So there are special requirements while polishing wafers are produced. Also during epitaxial process, the dopant will go into the atmosphere due to the high concentration of dopant in the wafer, from the part which is exposed to the atmosphere. This behavior will result in the contamination to the epitaxial layer, the unwanted dopant mixing into the epitaxial layer will lead to resistance deviation, and finally the Radium Resistance Variation (RRV) will exceed target value. This phenomenon is named Self-Doping[2-4]. In order to avoid this Self-Doping effect, while polishing wafer is produced, silicon dioxide is made on the back surface of wafers. This silicon dioxide will stop dopant from diffusing into the atmosphere to avoid Self-Doping

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phenomenon, but at the same time while silicon dioxide is made, thermal process will also work on defects gathering and geometry varying[5].

There are two main ways to make this silicon dioxide layer, HTO and APCVD[6], we will discuss the advantage and disadvantage if we choose which way to make the silicon dioxide layer, and compare the effect each way we take to make the silicon dioxide layer to the wafers.

2 Theories about making silicon dioxide layer

HTO Theories: The equipment we use to make silicon dioxide layer by HTO method is High Temperature Dispersing furnace. Wafers insert vertical on the carrier in the groove, there is small space between wafers, and the carrier will be pulled into the tube. Inside the tube the temperature is already higher than 900℃, the wafers will be kept in this tube for more than 8 hours, during this period, oxygen-oxygen and hydrogen-oxygen will be connected to the tube one after another. Oxygen in the tube will result in oxidation on both surfaces of the wafers. While we have oxygen and hydrogen in the tube at the same time we will have water, water will help to increase the rate of the oxidation. Different thickness of the layer is controlled by adjusting oxidation time, temperature and other parameters. After the oxidation process, wafers will be taken out from the tube then remove the silicon dioxide on the front surface of the wafers, because we can't polish the wafers with silicon dioxide on the surface.

APCVD Theories: The equipment we use to make silicon dioxide layer by APCVD method is APCVD furnace. Wafers will be laid on the surface of carrier horizontally, the backside of wafer contact the surface of carrier. Then the carrier will wander into and out the tube, during the wandering silane and oxide will be flow in, under the temperature about 500℃ silane will decompose and oxidized by oxygen into silicon dioxide. This process will take only 5 minutes and because one side of the wafers is protected by the carrier, there is only side will have silicon dioxide on the surface, so after APCVD, wafers are ready to be polished.

3 Experiments and Results

3.1 Comparison of thickness, thickness homogeneity and compactness of silicon dioxide layer between HTO and APCVD

We set our target of the thickness of silicon dioxide layer at 5100Å, after each process we measured 5 wafers from each process, each wafers measure 5 points as is shown in the Figure1. The results of thickness measurements are included in Table1.

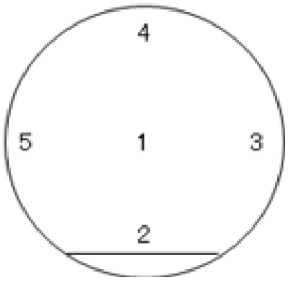


Figure1. Schematic of points chose to measure silicon dioxide layer thickness

From the table we find out that, HTO process is better than APCVD in homogeneity inside wafers and between wafers. The calculate formula is (max-min)/(2*average), from the result we can see homogeneity inside wafers from HTO process is always under 2%, the homogeneity between wafers in lower than 0.5%. The result shows by using HTO process we can get better homogeneity than APCVD. It is not strange to get this result, because HTO process is more stable than APCVD, a tube

filled with oxygen, 8 hours high temperature process, also the silicon dioxide layer comes from the wafer itself, the process conditions for all the wafers are quite the same, there conditions will help to get better homogeneity in making silicon dioxide layer. But in the APCVD process, silicon dioxide layer is deposited on the surface of wafers, within 5 minutes, the wafers in wandering in the tube, also the airflow of silane and oxygen may change from time to time, these conditions will all result in worse homogeneity in silicon dioxide layer.

Table 1. Thickness and thickness homogeneity comparison between APCVD and HTO

	No.	1	2	3	4	5	AVE	MAX	MIN	VAR
APCVD	1	5103	5211	5056	5024	5032	5085.2	5211	5024	1.84%
	2	5167	5272	5209	5057	5110	5163.0	5272	5057	2.08%
	3	5116	5251	5064	5117	5060	5121.6	5251	5060	1.86%
	4	5178	5277	5214	5213	5112	5198.8	5277	5112	1.59%
	5	5024	5118	4830	5050	5035	5011.4	5118	4830	2.87%
	Variation between wafers:									1.83%
HTO	1	5095	5142	5103	5016	5110	5093.2	5142	5016	1.24%
	2	5030	5126	5069	4983	5110	5063.6	5126	4983	1.41%
	3	5073	5140	5090	5011	5115	5085.8	5140	5011	1.27%
	4	5069	5155	5110	5020	5120	5094.8	5155	5020	1.32%
	5	5040	5165	5090	5021	5110	5085.2	5165	5021	1.42%
	Variation between wafers:									0.31%

Because silicon dioxide is only dissolved in hydrofluoric acid (HF), so we can use diluted HF to etch the silicon dioxide, if the compactness of silicon dioxide is different, with the same thickness of silicon dioxide, the dissolving time will be different. We can use eye inspection to check if there is silicon dioxide remained on the surface of wafers or not, if silicon dioxide remains, the surface will be hydrophilic, else will be hydrophobic. In order to control the dissolve rate, we diluted 49% HF with water (H_2O_2) at 1:14, and then inserted wafers from APCVD and HTO into the cassette together, then dropped the cassette into the solution. After etching some time, pulled the cassette up and checked the surface to see if it is hydrophilic or hydrophobic, etching time and surface status are recorded in Table 2. From the table we can see that, silicon dioxide from APCVD is much easier to remove, within 2 minutes the silicon dioxide is partly removed, and within 3 minutes, the silicon dioxide is completely removed. At this minute, silicon dioxide from HTO is still covered the whole surface of wafer. Continued on the experiments, we can see that silicon dioxide from HTO is partly removed at 8 minutes, and totally removed within 10 minutes.

Table 2. Etching time and surface status of APCVD and HTO wafers

Etching time	HTO	APCVD	NOTES
1min	Hydrophilic	Hydrophilic	
1.5min	Hydrophilic	Hydrophilic	
2min	Hydrophilic	Partly hydrophobic	Silicon dioxide partly removed
3min	Hydrophilic	Hydrophobic	Silicon dioxide totally removed
4min	Hydrophilic	Hydrophobic	
6min	Hydrophilic	Hydrophobic	
8min	Partly hydrophobic	Hydrophobic	Silicon dioxide partly removed
10min	Hydrophobic	Hydrophobic	Silicon dioxide totally removed

Repeated the above experiment, we got the same result. It is very normal to get this result, because with HTO process, silicon atoms near the wafer surface will be oxidized into silicon dioxide, this means oxygen atoms go into the gap between silicon atoms, this will make the density of silicon dioxide layer very high. For APCVD process, silicon dioxide is formed by silane and oxygen, and then deposited on the surface of wafers, the density is much lower than HTO.
In this part, we tried different dopant such as Arsenic, Antimony, Boron and Phosphorous, different orientation <111> and <100>, we always have the same result, it means that thickness homogeneity and compactness of silicon dioxide layer will only decided by the thermal process, wafer character will not impact on these items.

From section 2.1 we will know that HTO do a better job than APCVD, we will get better thickness homogeneity and compactness of silicon dioxide layer by using HTO.

3.2 Comparison of geometry parameter and defect gathering between HTO and APCVD

After ingots pulling, the ingots will be cooling down rapidly, stress will be remained inside the ingots, and also the ingots will experience a lot of processes such as slicing, edge grinding etc. During the mechanical process, stress and defects will be imported into the wafer. Stress is easier to release and small defects are easier to move to gathering during thermal process, the higher temperature (lower than 1100℃) thermal process is, the more stress will be released and smaller defects will gather together into bigger defects. Releasing the stress inside the wafer means geometry parameters BOW and WARP will change, especially WARP data; defect gathering means we will have bigger defects inside wafers that can be observed, these bigger defects will induce some defects to epitaxial layer which can't be accepted.

We prepared 40 wafers, including different dopant and different orientation, we measured the geometry data before thermal process, then 20 went to HTO and 20 went to APCVD, after that, measured them again, the tool we use here is ADE7200. We marked the result in Figure2: Warp data before and after HTO/APCVD process.

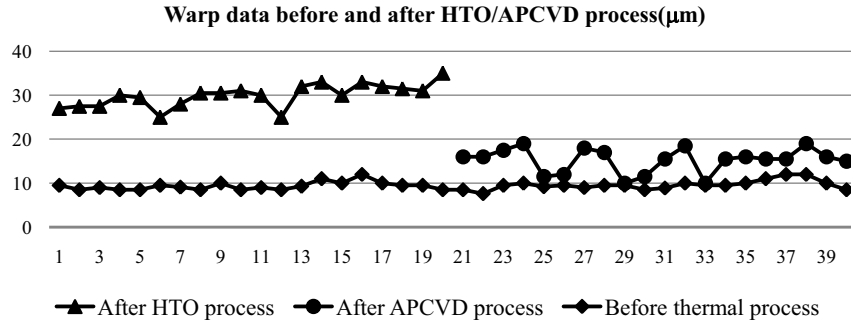


Figure2. Warp data before and after HTO/APCVD process

From the figure we can see that, before thermal process, the ◆ marks show us that all the 40 pcs wafers have quite the same WARP data, near 10 um. After thermal process we can see that, the ▲ marks and ●marks have quite different data, wafers with HTO process the WARP data changed much more than wafers with APCVD process, the average WARP data is near 32 um after HTO process, and the average WARP data is near 16 after APCVD process. Now we will know that APCVD will do better job in controlling WARP data, the experiment result is in accordance with theory analysis. We didn't observe any difference between different dopant nor different orientation.

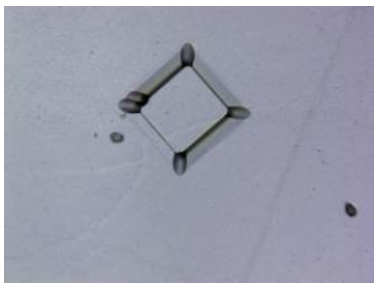
After measuring WARP data by ADE7200, we chose wafers with different orientation to observe defect, the wafers are from both APCVD and HTO. In order to make the observation easier, we polished all the wafers, and then used etching solution to etch them, and then through the microscope

we would get the results. The theory is that, after polishing, the surfaces of wafers are quite smooth, but defects still exist although can't be seen. In the etching solution, the defect area will be etched much faster than normal area free from defects, in this way, after etching process, we will get different surface topography on the wafer surface. As is mentioned above, the temperature of HTO process is higher we should have more defects observed from the wafers after this process. The coincidence is that the temperature for Oxide Induced Stacking Fault (OISF) is quite the same as HTO process, it means that, we may get much more defects after HTO process if there is small defects originally exist before HTO process. Figure3: Microscope photos after HTO process show us that, some wafers will be induced defects during HTO process, but some wafers are not, depend on if the smaller defects exist inside the wafers or not. For <100> and <111> we would get quite typical defect figure after HTO, for <100> orientation, square appeared, and for <111> orientation, triangle appeared. There figures are the combination of stacking faults and dislocation, at each vertex of the figure there are dislocations, and stacking faults will connect them together to make the square and triangle. These defects can't be seen after polishing, but during epitaxial process, these hidden defects will lead to epitaxial defects such as stacking faults and slip-line which can't be accepted.

From APCVD processed wafer, we did not observed any defects, because the temperature for APCVD is only 500℃ and the process time is only 5 minutes, far from the OISF temperature. Although smaller defects exist in the wafers, they do not have enough time and energy to move to get together. So after APCVD process we get photos all like the one from HTO which is free from defects.

<111>/<100> orientation free from defects

<111>orientation



<100> orientation

Dislocations and stacking faults combination

Figure3. Microscope photos after polishing with HTO process

This experiment means that HTO process is easier to induce defects, because of the high temperature and long time, but if we can control the smaller defects during the process before HTO process, we can also get defect free wafers after HTO. The original of the defects after HTO we observed is the smaller defects already existed inside the wafers.

From this section we will know that, due to the high temperature and long time in HTO process, WARP will deteriorate more than APCVD which has lower temperature and quite short process time. Also, if wafers have defects before HTO, HTO process will gather them together and make the combination harmful, but APCVD will not do this also due to the lower temperature and quite short process time.

4 Conclusion

From the above experiments, we know that HTO and APCVD, each process has its own advantage and disadvantage. HTO will do better job in the controlling of thickness homogeneity and compactness of silicon dioxide layer. APCVD is good at WARP controlling and defect inducing. One more advantage for APCVD wafers is that after thermal process, we do not need to remove the silicon dioxide layer with HF before polishing, which is necessary for HTO wafers.
In summary, which process we choose depend on the result we want and the usage for the product. In order to get better WARP, less defect and not much concern about the thickness homogeneity and compactness of silicon dioxide layer, we should choose APCVD. In order to get better thickness homogeneity and compactness of silicon dioxide layer, we should choose HTO. But if we want all of the advantages, we must control the level that defect and stress induced into the wafers very low before the HTO process, or else, HTO will destroy the wafers.

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