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USING NI PXI MODULES FOR DIGITAL SIGNAL PROCESSING MICROPROCESSOR TESTING

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Abstract. The article considers the implementation of the external memory interface based on National Instruments modular PXI equipment for environmental testing of digital signal processing (DSP) microprocessors. The block diagram of the developed device pointing out the advantages and disadvantages of this solution is provided. The block diagram of an improved external memory interface is also shown.

1 Introduction

One of the critical steps of the electronic equipment design for extreme environments is the initial evaluation and selection of system's components [1–15], even more so, for functionally complex ICs such as microprocessors and digital signal processors. The most important task here is to ensure the real operation mode of the chip at the highest operating frequency. The market of modern digital signal processing microprocessors is represented by a large number of various architectures and families. This makes the creation of a versatile and flexible system for testing different DSPs an especially relevant problem. The application of NI PXI-7841R reconfigurable I/O module for testing microprocessors is shown in [16]. This solution is based on the implementation of the direct memory access (DMA) controller interface. The main disadvantage of this approach is an irrational choice of the general interface. Not every DSP microprocessor contains a DMA interface, so it is necessary to implement the ability to download an executable program in the chip. Also, DMA controller interface can vary considerably depending on the specific model of the microprocessor under test. The usage of an external memory interface for testing DSP is devoid of these faults.

The article considers the implementation of the external memory interface with the reconfigurable I/O module NI PXI-7841R.

2 Equipment and software

The solution of the problem was implemented in NI LabVIEW 2010 programming environment with installed FPGA software module and modular devices' drivers.

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LabVIEW allows one to use visual programming language for mathematical processing of measurements results and generation of visual reports with graphs and statistical information. The external memory interface was developed on the basis of hardware and software system, as described in [16] with the use of such modular devices as:

- NI PXI-7841R module of an analog/digital I/O. This module provides the physical realization of the minimum environment required to complete the work of the DSP processor (timing system, interrupts, initialization, etc.), as well as measurement of logic voltage levels.
- NI PXI-4110 power supply module to set the voltage supply and control IC consumption current.

Modular devices are connected to a personal computer using PXI-1033 chassis.

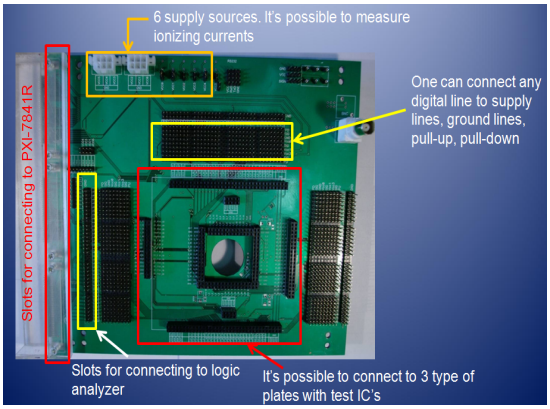

Figure 1. External view of the motherboard printed circuit board.

The main advantage of the hardware-software complex [16] is its versatility, which is achieved mainly by developing motherboard shown in Figure 1, which is connected to used NI PXI modules. Thus, in order to prepare for the testing of a new chip, only adapter board with standardized connectors must be manufactured. This approach significantly reduces the time and effort required to prepare the chip for testing. As an example, Figure 2 shows the adapter board for testing multiprocessing systems.

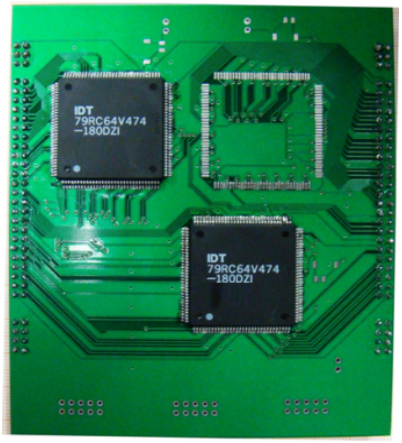

Figure 2. External view of the adapter printed circuit board with the multiprocessor's system under test.

3 Solution

An external memory interface is needed for connection of external RAM or ROM to a microprocessor. This memory may be used to load executable code into the test microprocessor and for storing intermediate data. In terms of processor performance, test implementation of this interface performs the following tasks:

- storage and loading of executable code;
- receiving and exchanging data with the microprocessor in real-time at full speed;
- high degree of standardization of this interface.

The program of external memory interface controller was created in the Host and FPGA modules. Application code that defines the configuration of the FPGA is developed on the host PC and then loaded into the FPGA. The LabView FPGA contains the most critical hardware blocks that require maximum performance during the interaction with the processor under test. The blocks that are developed in LabView Host do not require execution in real time. This module runs on a PC, so the speed of its implementation depends on the performance of the user's computer and programs priorities. The Host applications tasks include loading bin-file of the test firmware for the microprocessor in the FPGA module memory which is available to be read by the microprocessor and control operation of the entire application, analysis and logging test results.

Thus, to solve this problem it is necessary to implement block RAM on the FPGA Virtex-5 LX30, which is part of the NI PXI-7841R module, as well as physical realization of the external memory interface. Figure 3 shows a block diagram of the initialization memory unit.

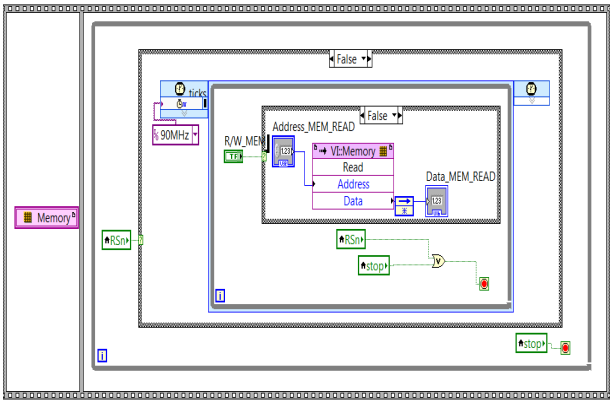

Figure 3. Block diagram of the initialization memory unit on the FPGA.

A block diagram of realization of the external memory interface is shown in Figure 4. The algorithm of this interface is the following sequence of operations:

- expectation of the start gate exchange cycle;
- definition of the type of the exchange cycle (read or write data). Simultaneously, the read address memory put up by a test processor and receiving data in the memory at the specified address with adjustable delay;
- depending on the type of exchange, either setting of information on the data bus (in the case shown in Figure 4), or reading the information and its recording in the RAM memory block occurs.

The advantages of the implemented interface are its high degree of versatility and flexibility, as well as the interface standard. The disadvantage is a relatively low speed. It was found during experiment that a stable work area of the interface is limited to

frequencies up to 40 MHz. This limitation is critical if it is impossible to change the frequency of the external memory interface of tested DSP. The analysis revealed that major delays are related to the usage of the Flat Sequence Structure, i.e. uncontrolled and non-fixed time delay in the transition "from frame to frame". It was decided to increase the speed of the interface by developing the improved structure.

Figure 5 is a block diagram of an improved external memory interface.

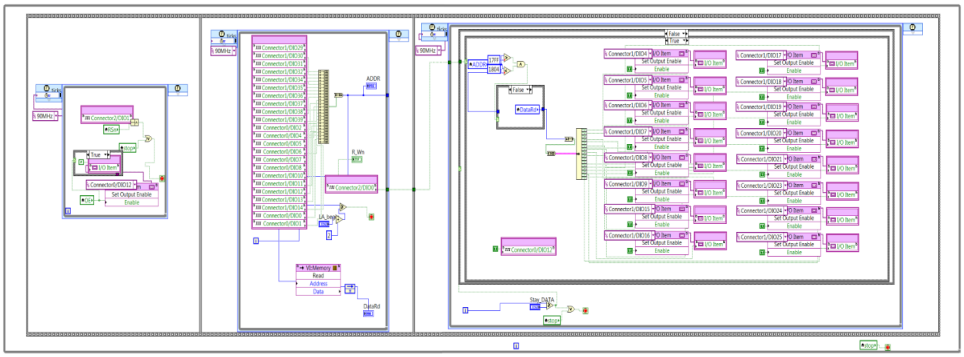

Figure 4. Block diagram of realization of the external memory interface. The read type of exchange.

The main feature of this implementation became the placing of the necessary operations in a single cycle using Time Loop Case Structure (so called State Machine) instead of using Flat Sequence Structure.

The RAM block mode became another implemented feature. Only one access operation to an array of memory cells (read or write) can be carried out at any given time. As a result, it was necessary to stop the operation of the processor in order to read the results of functional control test which the microprocessor stores in the RAM block. To solve this problem, the structure Array of Indicators has been used in parallel with the RAM module. This approach allows one to organize continuous information recording by the processor arbitration and read it from the FPGA module to the Host Module, while the test the microprocessor continues to operate at high speeds in the real time.

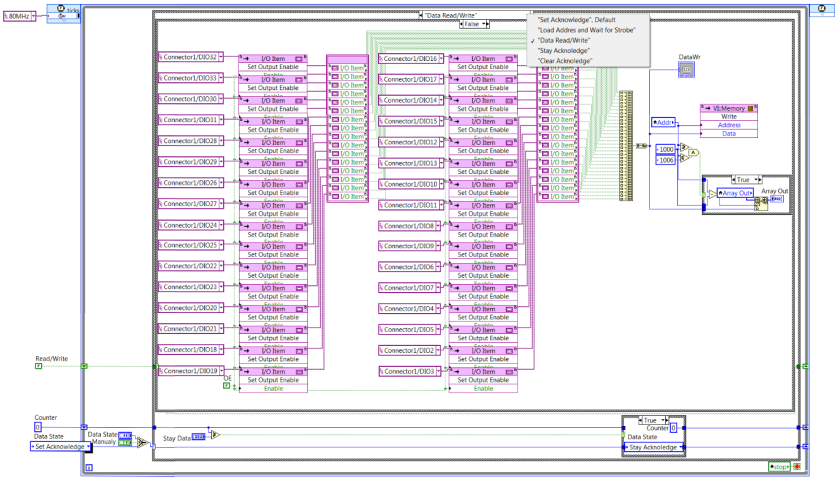

Figure 5. Block diagram of an improved external memory interface. The write type of exchange.

4 Experimental results

To test the efficiency of resulting external memory controller radiation behaviour researches of the DSP processor TMS320C50 (Texas Instrumenrs) were conducted in comparison with the use of DMA controller unit [16]. Functional control was consisted of testing internal memory blocks: 1) at maximum frequency (about 50 MHz), 2) using DMA interface (up to 100 kHz). During the experiment, it was found that functional failure doesn't revealed under exposure to extreme levels using DMA mode while the first method show functional failure that proves the inapplicability DMA mode as the sole means in testing processors under radiation fields.

Analyzing the results, we can conclude that the developed external memory controller provides more critical assessment of the radiation hardness of the DSP processor compared with the previously used DMA interface. This fact proves the significant impact of degradation time characteristics of inner units of DSP processors on the level of radiation hardness that occurs only at extreme frequencies of the scheme and the inability to obtain a critical assessment using a low-speed DMA interface

5 Conclusions

Developed external memory controller interface was successfully used for testing a variety of microprocessors which include general purpose microprocessors (IDT79RC64474 with MIPS architecture, AT697F with the SPARC architecture, Intel 80386, etc.) and DSPs (processor's family by Texas Instruments - TMS320C2x, TMS320C3x, TMS320C5x , TMS320C2xx, TMS320C5000, TMS320C6000 and many others), this unit requires minimal setup that significantly reduces the time of preparation.

Note that this implementation allows us to significantly increase the speed (up to 100 MHz) and doesn't contain uncontrolled time delays. The minimum time interval is equal to the period of the clock signal for the Time Loop cycle. At the same time, this implementation of an external memory interface keeps such advantages as flexibility, standardization and flexibility of the developed external memory interface.

Acknowledgements

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References

[1] A. Y. Nikiforov, P. K. Skorobogatov, A. N. Egorov, D. V. Gromov, Russian Microelectronics **43**(2), 133 (2014) doi: 10.1134/S1063739714020073

[2] M. P. Belova, D. V. Pechenkina, A. Y. Borisov, L. N. Kessarinskiy, D.V. Boychenko, 2015 International Siberian Conference on Control and Communications (SIBCON), 7146995 (2015) doi: 10.1109/SIBCON.2015.7146995

[3] A. G. Petrov, A. L. Vasil'ev, A.V. Ulanova, A. I. Chumakov, A.Y. Nikiforov, Central European Journal of Physics **12** (10), 725 (2014) doi: 10.2478/s11534-014-0503-6

[4] L. N. Kessarinskiy, D. V. Boychenko, A. Y. Nikiforov, Russian Microelectronics **41**(4), 251 (2012) doi: 10.1134/S1063739712040075

[5] I. O. Loskutov, A. B. Karakozov, P. V. Nekrasov, A. Y. Nikiforov, 2015 International Siberian Conference on Control and Communications (SIBCON), 7147128 (2015) doi: 10.1109/SIBCON.2015.7147128

[6] A. O. Akhmetov, D. V. Boychenko, D. V. Bobrovskiy, A. I. Chumakov, O. A. Kalashnikov, A. Y. Nikiforov P. V. Nekrasov, Proceedings of the International Conference on Microelectronics (ICM), 329 (2014) doi : 10.1109/MIEL.2014.6842156

[7] G. V. Chukov, V. V. Elesin, G. N. Nazarova, A. Y. Nikiforov, D. V. Boychenko, V. A. Telets, A. G. Kuznetsov, K. M. Amburkin, IEEE Radiation Effects Data Workshop, 7004589 (2014) doi: 10.1109/REDW.2014.7004589

[8] A. S. Artamonov, A. A. Sangalov, A. Y. Nikiforov, V. A. Telets, D. V. Boychenko, IEEE Radiation Effects Data Workshop, 7004600 (2014) doi : 10.1109/REDW.2014.7004600

[9] A. N. Egorov, A. I. Chumakov, O. B. Mavritsky, A. A. Pechenkin, D. V. Savchenkov, V. A. Telets, A. V. Yanenko, IEEE Radiation Effects Data Workshop, 7004570 (2014) doi: 10.1109/REDW.2014.7004570

[10] I. I. Shvetsov-Shilovskiy, P. V. Nekrasov, A. V. Ulanova, A. A. Smolin, A. V. Sogoyan, 2015 International Siberian Conference on Control and Communications (SIBCON), 7147282 (2015) doi: 10.1109/SIBCON.2015.7147282

[11] A. B. Boruzdina, A. A. Orlov, A. V. Ulanova, N. G. Grigor'ev, A. Y. Nikiforov, 2015 International Siberian Conference on Control and Communications (SIBCON), 7147007 (2015) doi: 10.1109/SIBCON.2015.7147007

[12] D. V. Bobrovskii, O. A. Kalashnikov, P. V. Nekrasov, Russian Microelectronics **41** , 226 (2012) doi: 10.1134/S1063739712040038

[13] P. V. Nekrasov, A. A. Demidov, O. A. Kalashnikov, Instruments and Experimental Techniques **52**, 196 (2009) doi: 10.1134/S0020441209020092

[14] Jin Ming Zhanga and He Zhang, MATEC Web of Conferences **44**, 01030 (2016) doi: 10.1051/matecconf/20164401030

[15] Ning Ma, Shaojun Wang, Syed Mohsin Ali, Xiuhai Cui and Yu Peng, MATEC Web of Conferences **45**, 05001 (2016) doi: 10.1051/matecconf/20164505001

[16] V. A. Marfin, P. V. Nekrasov, O. A. Kalashnikov, K. A. Kagirina, 2015 International Siberian Conference on Control and Communications (SIBCON), 7147142 (2015) doi: 10.1109/SIBCON.2015.7147142