

NI BASED SYSTEM FOR SEU TESTING OF MEMORY CHIPS FOR AVIONICS

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Abstract. This paper presents the results of implementation of National Instrument based system for Single Event Upset testing of memory chips into neutron generator experimental facility, which used for SEU tests for avionics purposes. Basic SEU testing algorithm with error correction and constant errors detection is presented. The issues of radiation shielding of NI based system are discussed and solved. The examples of experimental results show the applicability of the presented system for SEU memory testing under neutrons influence.

1 Introduction

The problem of Single Event Upset (SEU) in memory under influence of atmospheric neutrons and also under secondary neutrons of physics facilities is well known [1–3]. This problem is increasing along the feature sizes of critical electronic components (processors, memories) of control systems became smaller and demands a high level of attention [4–8], especially referring to avionics safety.

Solving of the problem of SEU in memory under influence of neutrons is in prediction of the electronic components sensitivity to neutron irradiation [9] and in implementation of error correction methods utilizing the level of sensitivity. To obtain sensitivity parameters one should perform radiation tests using experimental facilities, such as proton accelerators and neutron generators. One of these facilities is the neutron generator in MEPhI (Moscow, Russia) which can produce neutron fluxes of energy about 2 MeV or 14 MeV.

Memory is an essential component of modern control systems, in which memory is usually represented as is and also as a part of processors, programmable logic etc. Considering SEU, the memory seems to be the most sensitive part of the systems, due to its highest integration level. Therefore, we have chosen memory chips as the object of our experiments.

To perform functional control of memory chips during SEU tests the special test algorithms should be used. The algorithms should include an information safety check in each memory cell, and also an operability check of each cell. The latter is important to be sure that the error of the cell is the SEU rather than constant failure (imprinting effect) due to total ionizing dose (TID). The special algorithm and the hardware were developed on the basis of National Instrument (NI) platform and NI LabVIEW 11.0 software.

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Another part of the work is to supply safety operation of NI based system under influence of neutron fluxes of neutron generator. The distance between memory chip and NI based test system is about 2 meters and could not be larger taking into consideration the length of standard cables. At this distance the level of irradiation is rather high to leave it unsolved: the risk of system failure due to neutron flux and total dose irradiation should be decreased to negligible levels. Keeping in mind the high penetration ability of neutrons there are only two ways to decrease the level of irradiation: (1) to increase the distance between the system crate and the neutron source, which is impossible for the length of cables, and (2) to mount an appropriate shield between them, which was one of the tasks of this work.

2 Hardware and software

The special algorithm and the LabVIEW software for memory chip SEU testing along with simultaneous operability check of each memory cell was developed using NI LabVIEW 11.0. The software was developed to be running on the NI PXI platform which was based on PXI-1033 chassis, or so called “crate”, with a field-programmable gate array (FPGA) module PXI-7951R supplemented with an adapter module NI 6581 and a PXI-4110 power supply which all together were “the measuring unit”.

The exterior view of the VI toolbox managing operational modes of the memory chip under test is shown in Figure 1. The parametric control panel allows to command two power supply channels of memory chip under test, measure supply current and detect single event latchup (SEL) in each channel separately. The functional control panel allows choosing a functional test pattern, performing writing and reading operations start and stop SEU test and indicating the number of both SEU and constant errors. At the bottom of the VI toolbox an operator can input the filenames for log files.

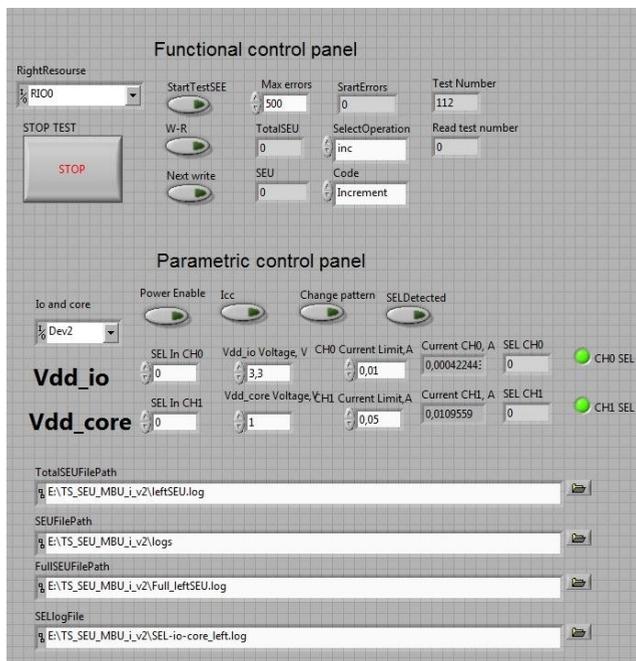


Figure 1. The exterior view of the VI toolbox managing operational modes of the memory chip under test.

The measuring unit was connected to the memory chip under a test with a standard cable providing suitable frequencies for the test. The controlling computer was located 7 meters away from the measuring unit, in a safe area where no irradiation was available.

3 Test algorithm

The block diagram shown in Figure 2 describes the special algorithm for SEU testing developed to control both the SEU under neutron irradiation and constant hard errors in each memory sell of the memory chip under test. The algorithm includes the following steps:

- 1) Writing the test pattern P2 which is inverse to the initial pattern P1.
- 2) Reading and comparing the read data with the pattern P2 to evaluate constant errors.
- 3) Writing the initial test pattern (P1) to the memory chip.
- 4) Reading and comparing the read data with the pattern P1 to evaluate constant errors.
- 5) Writing the initial test pattern (P1) to the memory chip.

SEU testing starting from the address 0x0 up to the maximum logical address performing the following operation for each cell in the logical word:

- 1) reading the logical word and comparing the read data with the corresponding data W1 from pattern P1 for preliminary SEU registration;
- 2) writing the data W2 which is inverse to W1 to the same logical word;
- 3) reading the same logical word again and comparing the read with W2 to evaluate constant hard errors (imprinted W1 data) in each bit;
- 4) writing W1 to the same logical word;
- 5) reading the same logical word again and comparing the read data with W1 to evaluate constant hard errors (imprinted W2 data) in each bit;
- 6) calculating true SEU data in each bit using preliminary SEU data excluding imprinted bits evaluated in intermediate steps.

The selection of initial test pattern is essential. Plain patterns such as “all ones” or “all zeroes” are not effective for detecting errors in an address decoder on the memory chip. The better choice is random pattern but this kind of pattern is sophisticated for hardware implementation. The compromise is the so called “incremental” pattern which is irregular enough to reveal address decoder problems and at the same time regular enough to be implemented to hardware using simple counter registers. The view of the fragment of the VI block diagram shown in Figure 3 performs the algorithm described above.

The SEU testing is looped until the appropriate number of SEUs will be counted.

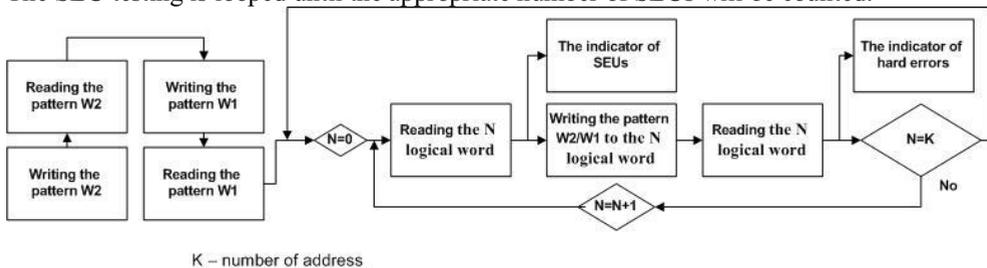


Figure 2. The algorithm of SEU testing for memory chip, which allows to reveal constant or hard errors.

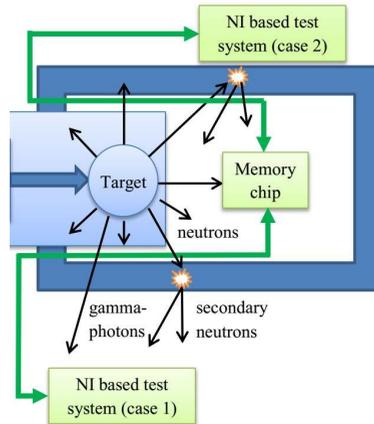


Figure 5. The shielding of the target and the memory chip under test leads to producing secondary neutrons and gamma-photons, but the flux of primary neutrons becomes significantly less.

The estimation of neutron fluxes and the TID in the place of the NI crate disposal have been performed taking into consideration both primary and secondary irradiation. The calculations were performed using MCNP software utilizing Monte Carlo codes. Calculations were performed step by step starting with a very simple environment model (dotted neutron source approximation) to a complete environment model taking into consideration the materials and the geometry of the tritium target, approximated geometry and material of the memory chip mounted on the printed circuit board and the steel shield.

The results of calculations showed that the fluxes of secondary neutrons and gamma-photons on the memory chip under test are not negligible. The neutron flux increase, in the energy range from 1 MeV to 14 MeV, was about 8% on account of the geometry and the material of the target, while the contribution of the memory chip material and the printed circuit board was about 5%, and the contribution of steel shield was about 0.5%. The corresponding decreases of 14MeV neutrons flux on the memory chip are about 11%, 6% and 1%. Therefore, the aggregated uncertainty of the neutron flux of 14 MeV on the memory chip under test is less than 20%.

The neutron flux on the NI crate was calculated by taking into account that the typical neutron flux on the memory chip needed during SEU test experiment is about 10^{11} neutron/cm². Keeping in mind that the distance from the neutron source is essential for the neutron flux we considered two cases (see Figure 5) of the geometry allowed by the length of the cable between the NI crate and the memory chip under test: (1) the NI crate is situated as far as possible from the target of the neutron generator, but still in the “shadow” created by the steel shield, and (2) the NI crate is situated about in the middle of a “shadow” but very close to the walls of the steel shield.

The results of calculations of the neutron fluxes on the NI crate under different conditions are shown in the Figure 6. As it follows from the calculation results the steel shield effectively absorbs initial 14 MeV neutrons irradiation but at the same time it becomes the source of a huge amount of low energy neutrons especially with the energy of less than 1 MeV, but these kinds of particles can not produce any upsets in electronics and may be assumed harmless. The place of disposal do not play essential role while using the steel shield, but case (1) is more effective for low energy neutrons, because in this case the NI crate is situated more far from the steel shields which is the source of secondary neutrons in this case.

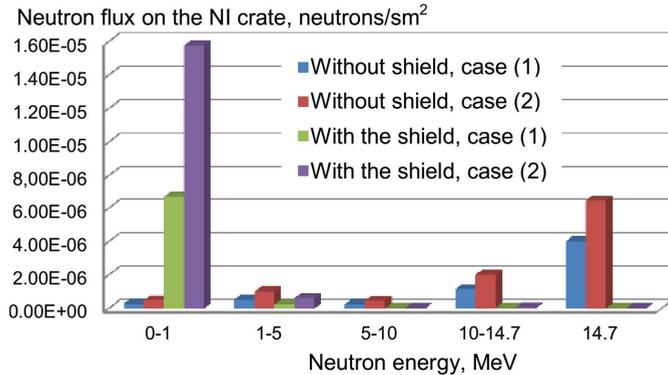


Figure 6. The results of calculations of the neutron fluxes on the NI crate under different conditions.

The TID on the memory chip was also calculated in correspondence to the flux of about 10^{11} neutron/cm². According to the calculations the TID level is about 20 rad per one experiment which is quite a negligible value for memory chips. The TID level in the place of NI crate disposal was several orders of magnitude less than on the memory chip being tested, which allows us to use the NI crate for thousand experiments without any fears of TID failure.

Developed external memory controller interface was successfully used for testing a variety of microprocessors which include general purpose microprocessors (IDT79RC64474 with MIPS architecture, AT697F with the SPARC architecture, Intel 80386, etc.) and DSPs (processor's family by Texas Instruments - TMS320C2x, TMS320C3x, TMS320C5x, TMS320C2xx, TMS320C5000, TMS320C6000 and many others), this unit requires minimal setup that significantly reduces the time of preparation.

Note that this implementation allows us to significantly increase the speed (up to 100 MHz) and doesn't contain uncontrolled time delays. The minimum time interval is equal to the period of the clock signal for the Time Loop cycle. At the same time, this implementation of an external memory interface keeps such advantages as flexibility, standardization and flexibility of the developed external memory interface.

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5 Experimental results

The NI based SEU test system was verified during several experiments with two types of memory chips (Table 1) under the influence of 14 MeV neutrons. Both memory types had supply voltage of 5V.

Table 1. Memory chips used in the experiment.

Type	Manufacturer	Size	Feature size
AS7C4096	Alliance	512Kx8	0.18 um
K6X1008C2D	Samsung	128Kx8	0.13 um

The results of SEU tests (Table 2) show an applicability of NI based SEU test system for the experiments of that sort. The numbers of SEU are in good correlation with measured neutron fluxes. No constant errors N_{CE} in memory cells were observed during the experiment, it agrees with negligible levels of TID.

Table 2. Results of SEU tests

Type of memory chip	Number of sample	Neutron flux	N_{SEU}	N_{CE}
AS7C4096	1	2.20E+09	251	0
	2	5.48E+09	535	0
	3	5.19E+09	496	0
K6X1008C2D	1	8.02E+09	101	0
	2	7.70E+09	102	0
	3	7.54E+09	78	0

6 Implementation and its prospects

The automated NI based system developed in this work allows performance of SEU tests in memory chips during neutron irradiation. The appropriate shielding was developed to minimize total dose and neutron flux influences on NI crate. This NI based system was successfully implemented at JSC “ENPO SPELS” and NRNU MEPHI (Moscow). Future plans are to elaborate the control logic for dynamic types of memory.

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