Influence of Optimization of Process Parameters on Threshold Voltage for Development of $HfO_2/TiSi_2$ 18 nm PMOS

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Abstract. Manufacturing a 18-nm transistor requires a variety of parameters, materials, temperatures, and methods. In this research, HfO_2 was used as the gate dielectric ad TiO_2 was used as the gate material. The transistor $HfO_2/TiSi_2$ 18-nm PMOS was invented using SILVACO TCAD. Ion implantation was adopted in the fabrication process for the method's practicality and ability to be used to suppress short channel effects. The study involved ion implantation methods: compensation implantation, halo implantation energy, halo tilt, and source–drain implantation. Taguchi method is the best optimization process for a threshold voltage of $HfO_2/TiSi_2$ 18-nm PMOS. In this case, the method adopted was Taguchi orthogonal array L9. The process parameters (ion implantations) and noise factors were evaluated by examining the Taguchi's signal-to-noise ratio (SNR) and nominal-the-best for the threshold voltage (VTH). After optimization, the result showed that the VTH value of the 18-nm PMOS device was -0.291339.

1 Introduction

"Metal–oxide–semiconductor field-effect transistor" or "MOSFET" is a very prevalent type of transistor. It is unique because it entails very little current to turn on (less than 1.0 mA) yet delivers a much higher current to a load (10.0mA to 50.0A or more). This transistor is cheap yet flexible and reliable; it can be considered the key active component in all modern electronics.

Over a billion of individually packaged MOSFETs (known as discrete) are manufactured every year in order to meet the increasing demands for ICs from electronic companies. This in turn reduces the price of every chip. Smaller-sized ICs allow more chip transistor per wafer to be produced. Scaling down the metal-oxide-semiconductor, according to Moore's law, have been improving at sensational level [1], leading to massive improvement in the operation and performance of MOSFET. The transistor's faster digital switching can save time, energy, and power, improving the operation of transistors. Additionally, the reduced size of MOSFET has not only proportionally reduced the

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dimensions of all devices dimensions in terms of the channel length, channel width, and oxide thickness but has also affected the transistor's doping.

However, smaller-sized transistors are more difficult to develop. The process requires prolonged hours, concentration, and consistency to enable the transistor to function efficiently. To control the threshold voltage is the main task in produce a nanoscale transistor. If the optimum VTH value is not achieved, doping fluctuations will occur and the whole system of the device will be affected [2].

In this research, dopant ions such as phosphorus, boron and arsenic are used for ion implantation. Many process parameters can influence an 18nm-PMOS fabrication such as halo implantation, halo implantation energy, halo tilt, source/drain implantation, VTH adjustment implantation, compensation implantation, and VTH adjustment energy. Manipulating the dose, energy, and rotation of the implants will alter the profile and electrical characteristics of the devices [3]. The aim was to obtain one of the most optimum VTH value for MOSFET. In this research, HfO_2 was used as gate oxide. Combination HfO_2 and $TiSi_2$ is to obtain the highest value of ION/IOFF ratio and the lowest value of sub-threshold leakage current (IOFF). The purpose is to render this device suitable for low power application [4]. Nevertheless, we attempted to discover the best combination of four process parameters that can yield the optimal value of VTH.

This Taguchi's orthogonal array method evaluates the entire process parameters with only a few experiments and noise factor in order to get the optimal process parameters [5]. The aim of the current work is to meet the threshold voltage in the ITRS 2011 specification for a 18-nm gate length PMOS transistor with a VTH value of 0.302V [6]. The Taguchi's robust design is a powerful statistical tool often used in industrial process optimization and analysis. The method can be applied to the design of high quality systems without increasing costs, and it can also reduce the time for the development process [7].

2 Method and materials

2.1 Process steps and device

The development of $HfO2/TiSi_2$ 18-nm PMOS transistor was fabricated using Virtual Wafer Fabrication (VWF) SILVACO TCAD. A p-type (boron doped) silicon bulk sampled is used with <100> alignment and a doping concentration of 7×10^{14} atoms/cm^2. The next process was to develop retrograde N well. In this process a 200 Å oxide layer was growing on the top of the substrate at high temperature of 970^{o}C for 20 minutes. The following step was to generate a shallow trench isolation (STI) of 130-Å thickness. This annealing process takes 25 minutes at temperature 900°C in dry oxygen. By applying a low pressure chemical vapour deposition process (LPCVD), a 1500-Å nitride layer was deposited on top sample of the oxide layer. Photoresist layer was then deposited on the wafer and through a reactive ion etching (RIE) process the unnecessary part at the top of the STI area was etched away. After the desired depth of STI was achieved, an oxide layer was grown on the trench sides to eliminate any impurities from entering the silicon substrate. To eliminate any extra oxides on the substrate surface, the Chemical mechanical polishing (CMP) was then applied. The STI was then annealed for 15 minutes at a temperature of 850°C to develop a phosphor silicate glass (PSG) at the top of the substrate followed by oxide and nitride pad. The sacrificial oxide layer was formed once the STI was completely annealed and etched accordingly to remove defects on the surface.

The next step was the crucial process of growing the gate oxide. The gate oxide layer was grown by exposing the silicon wafer to dry oxygen for a very short time of 10ms at 850°C. This condition served to ensure that a 1.1-nm thickness of gate oxide (TOX) was

grown. Once the substrate was annealed, boron difluoride (BF2) was implanted at the N-well active area to adjust the VTH of the device. The dosage of boron applied was 1.6757777×10^7 atoms/cm^2 whereas the energy used was 5KeV with a tilt angle of 7°. Among the channel regions, on the top of the silicon bulk was the deposition process of Hafnium Dioxide (dielectric permittivity HfO_2, εopt = 22) as dielectric material. The length of the high-K material was scaled and adjusted to get 18nm same value as the gate length of the transistor. Thus, the process done for Titanium Silicide ($TiSi_2$) deposited on the top of HfO_2, and followed by a Halo implantation process with implanted phosphor as a dopant at a dose of 5.581×10^{13} atom/cm^2 with an angle tilted at 30° and halo energy of 290KeV.

The next step was to form the sidewall spacer using a chemical vapour deposition (CVD) process, a 0.047-µm silicon nitride layer was deposited and was etched for the same deposition thickness. Then, a source-drain implantation process was conducted at 7° with boron as a dopant at a density of 5.556666×10^{13} atom/cm^2, with 11KeV implantation energy. The next step was to develop a 0.3 µm layer of boron phosphor silicate glass (BPSG). This layer acted as the pre metal dielectric (PMD). In the same way, the annealing process was performed at the wafer to strengthen the structure at 850°C. The final process of wafer was to implant the compensation a phosphor dose of 2.5×10^{13} atom/cm^2 at 60KeV implantation energy. The beam was tilted at 7°. Finally, the aluminum layer was etched accordingly after it was deposited on the top of structure to form metal contacts for the source and drain. This point completed the production of the 18-nm PMOS transistor (Figure 1 and Figure 2).

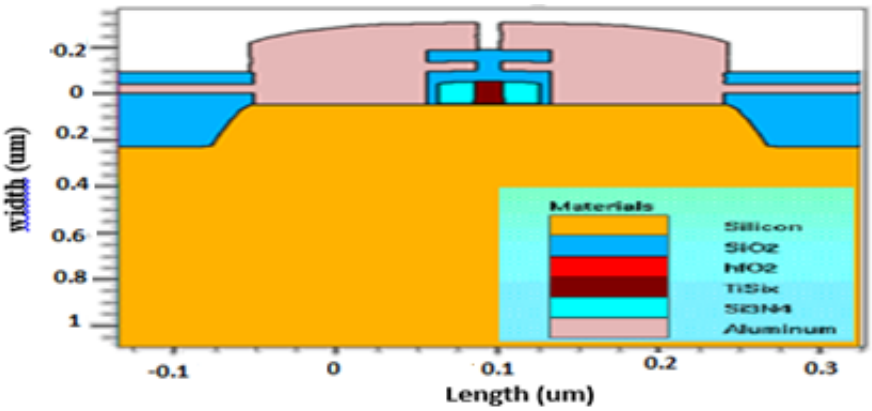

Fig. 1. A complete $HfO_2/TiSi_2$ 18nm PMOS.

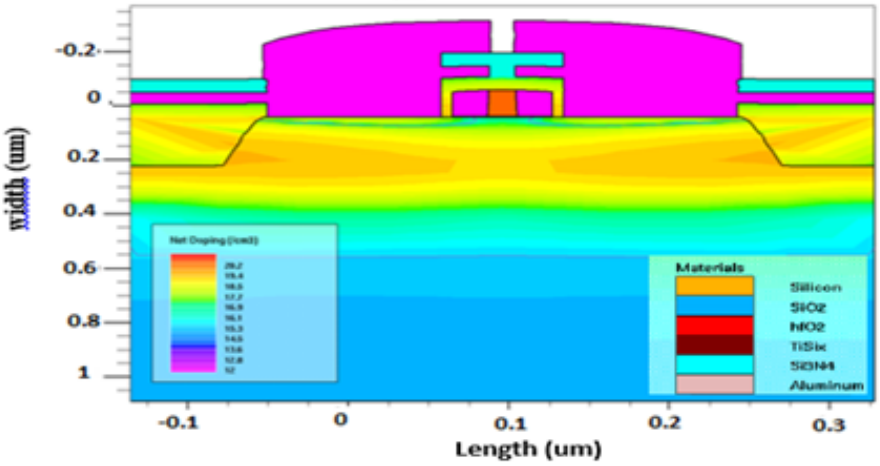

Fig. 2. A complete $HfO_2/TiSi_2$ 18nm PMOS doping profile.

2.2 Taguchi orthogonal L9 array method

In this L9 Orthogonal, the process parameters were Compensation Implantation, Halo Implantation Energy, Halo tilt and Source-Drain Implantation. Whereas, the temperatures of phosphorus silicate glass (PSG) and boron phosphorus silicate glass (BPSG) were the noise factors. In this study, we carried out three experiments of different combination of process parameters but with the same noise factors. The purpose was to obtain the best combination of process parameter with a good VTH value. The following section reports the best result of process parameters.

3 Result

From the result of the three experiments, this experiment was selected because it shows a good VTH value from the combination of different four process parameters and noise factors as tables below.

Table 1. Process Parameters and Levels.

Symbol	Process Parameter	Unit	Level 1 [L1]	Level 2 [L2]	Level 3 [L3]
A	Compensation Implantation	atom/ cm^3	14.871000e13	14.875000e13	14.879000e13
B	Halo Implantation Energy	KeV	294	295	296
C	Halo Tilt	Degree	30	32	34
D	Source-Drain Implantation	atom/ cm^3	5.394000 e13	5.400000 e13	5.406000 e13

Table 2. Noises Factor and levels.

Symbol	Noise Factor	Unit	Level 1	Level 2
X	PSG	°C	850	851
Y	BPSG	°C	850	851

3.1 Analysis of 18-nm PMOS device

The Taguchi Orthogonal L9 array projected thirty-six simulation runs from the nine experiments. The completed result for VTH data is shown in Table 3. Two control factors were considered: dominant factor and an adjustment factor. A signal-to-noise ratio (SNR) analysis was used to identify the optimal process parameters in this experiment. A larger S/N ratio corresponds to better performance [8].

Table 3. VTH Values for 18-nm PMOS Device.

EXPERIMENT NO	VTH1 X_1Y_1	VTH2 X_1Y_2	VTH3 X_2Y_1	VTH4 X_2Y_2
1	-2.51E-01	-2.39E-01	-2.49E-01	-2.37E-01
2	-3.16E-01	-3.04E-01	-3.14E-01	-3.02E-01
3	-5.85E-01	-5.42E-01	-5.76E-01	-5.84E-01
4	-2.77E-01	-2.66E-01	-2.75E-01	-2.64E-01
5	-4.12E-01	-3.98E-01	-4.10E-01	-3.95E-01
6	-3.56E-01	-3.43E-01	-3.54E-01	-3.41E-01
7	-1.27E-01	-1.31E-01	-1.28E-01	-1.33E-01
8	-2.85E-01	-2.74E-01	-2.83E-01	-2.72E-01
9	-3.62E-01	-3.54E-01	-3.61E-01	-3.52E-01

In this research, the VTH of the 18-nm device indicates the characteristics of nominal-the-best quality [8]. This characteristic was selected to obtain a VTH closer to -0.302V for 18-nm transistor which is the value predicted by International Roadmap of Semiconductor (ITRS) 2011. The formula of SNR (nominal-the-best), η can be expressed as [9]:

$$\eta = 10\mathrm{Log}_{10}\left[\frac{\mu^2}{\sigma^2}\right] \quad (1)$$

and

$$\sigma^2 = \frac{\sum_{i=1}^{n}(Y_i - \mu)^2}{n-1} \quad (2)$$

Where n is the number of tests, Y is the experimental value of the VTH, μ is mean, and σ is variance. The dominant factor and the adjustment factors need to be considered in SNR of category Nominal-the-Best. By applying the formulae (1) and (2), the SNR (η) for the PMOS device was calculated and the results are shown in Table 4.

Table 4. Mean, Variance and S/N Ratio for PMOS Device.

Experiment No.	Mean	Variance	SNR (Mean)	SNR (Nominal-the-best)
1	-2.44E-01	4.68E-05	-1.22E+01	3.11E+01
2	-3.09E-01	4.60E-05	-1.02E+01	3.32E+01
3	-5.72E-01	4.22E-04	-4.86E+00	2.89E+01
4	-2.70E-01	4.28E-05	-1.14E+01	3.23E+01
5	-4.04E-01	7.21E-05	-7.88E+00	3.35E+01
6	-3.49E-01	5.66E-05	-9.15E+00	3.33E+01
7	-1.30E-01	7.83E-06	-1.77E+01	3.33E+01
8	-2.79E-01	4.77E-05	-1.11E+01	3.21E+01
9	-3.57E-01	2.38E-05	-8.94E+00	3.73E+01

The mean SNR for the nine experiments were calculated and plotted in Figure 3. The larger the SNR, the better the quality characteristic for the VTH. From Figure 3, we can identify which level of the process parameters is the dominant factor and adjustment factor for this experiment. The dominant factor has the biggest effect on SNR and the adjustment factor poses the largest effect on mean and the smallest effect on SNR. From the graph, we can see that the dominant factor appears for compensation implantation (A3), followed by halo tilt (C2), source-drain implantation (D1), and halo implantation energy (B3), whereas halo implantation energy is the adjustment factor.

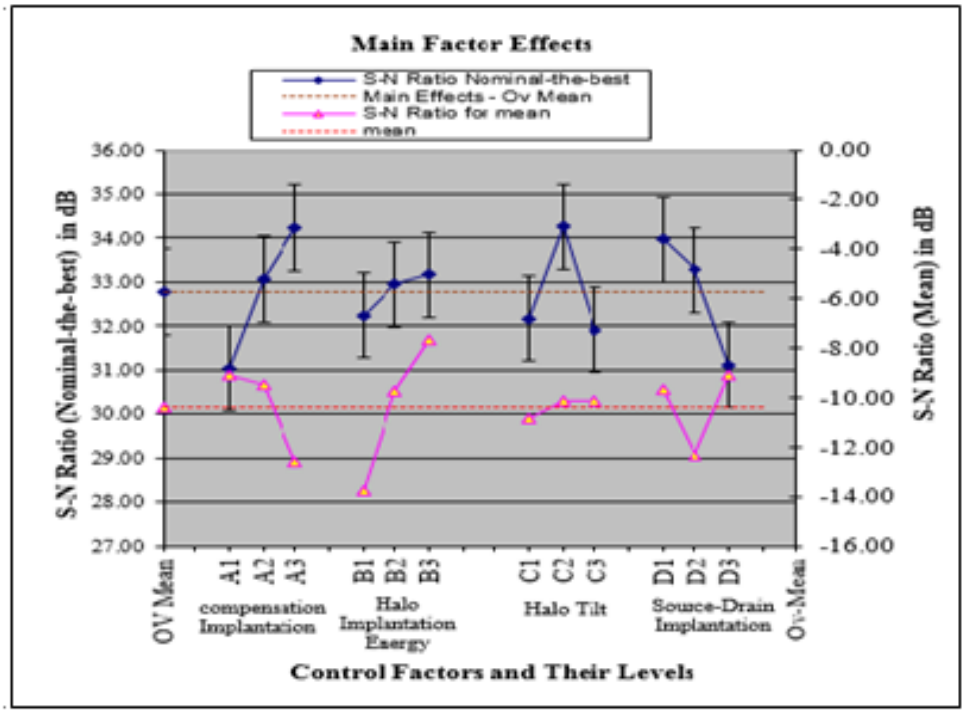

Fig. 3. Graph of S/N ratio (Nominal-the-Best).

3.2 Analysis of variance (ANOVA)

ANOVA is one of the most common statistical techniques to determine the percentage contribution of the optimum combination of the process parameters for the device. This analysis can also be used to identify which of the control factor has the most effective to the VTH. The highest percentage of SNR has the greatest effect on the stability of the VTH and hence the responsible parameter will be the dominant factor. From Table 5, compensation implantation has the most effect on the VTH of 18-nm PMOS (39% SNR). Hence, compensation implantation is the dominant factor. The source-drain implantation poses a factor effect on SNR of 33%, which is the second largest effect after compensation implantation. Halo tilt poses a percentage of SNR of 25% and 4% of SNR for halo implantation energy. We can also identify the adjustment factor from this table, which is the halo implantation energy. It has the largest effect on mean, (58.62%) and the smallest effect on SNR of (4%).

Table 5. Result of ANOVA for 18nm PMOS Device.

Symbol	Process Parameter	Factor Effect on SNR (%)	Factor Effect on Mean (%)
A	Compensation Implantation	39	22.29
B	Halo Implantation Energy	4	58.62
C	Halo Tilt	25	0.90
D	Source-Drain Implantation	33	18.20

3.3 Confirmation of optimum factor

The above results shows that halo implantation energy is suitable for the optimal design of the device because the parameter serves as the adjustment factor. The dose can be adjusted from 294KeV to 296KeV until we achieved the threshold voltage closest to the nominal or target value, which is -0.302 as required by ITRS 2011 for 18 PMOS device. Again, the final experiment must be conducted using the final value of process parameters as shown in Table 6. This time only one simulation was run with the same noise factors such as PSG temperature and BPSG temperature.

Table 6. Best Setting of Process Parameters.

Symbol	Process Parameter	Unit	Level	Best Value
A	Compensation Implantation	atom/cm^3	3	14.879000e13
B	Halo Implantation Energy	KeV	1	294
C	Halo Tilt	Degree	2	32
D	Source-Drain Implantation	atom/cm^3	1	5.394000e13

From the result of the best setting the process parameters, we obtained the values as shown in Table 7. Table 7 compares the VTH before optimization and after optimization, as well as the ITRS value. After optimization under X2Y2, the value of VTH was -0.291339. This value was selected as the final value of VTH after optimization because the value is within to ITRS 2011 requirements of -0.302 ± 12.7% [10, 11].

Table 7. Final Result of VTH after Confirmation Experiment.

Experiment No	Before Optimization (Volt)	After Optimization VTH 4 (Volt) X_2Y_2	ITRS 2011 VTH (Volt)
1	-0.32047	-0.291339	-0.302

4 Summary

The optimum solution in achieving the best level of process parameters in the development of VTH for $HfO_2/TiSi_2$ 18 nm PMOS transistor was successfully predicted by using Taguchi L9 Orthogonal array. The compensation implantation dose was identified to be the dominant factor, and halo implantation energy was identified as the adjustment factor in this device. Both process parameters are the most effective parameters with respect to a threshold voltage (VTH) of -0.291339V.

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