MATEC Web of Conferences **78**, 01017 (2016) DOI: 10.1051/matecconf/20167801017
IConGDM 2016

Process Parameters Optimization of 14nm MOSFET Using 2-D Analytical Modelling

Z.A. Noor Faizah[1,*], *Ibrahim* Ahmad[1], *P.J.* Ker[1], *Y.* Siti Munirah[1], *R.* Mohd Firdaus [1], *E.* Md. Fazle[1], and *P. S.* Menon[2]

[1]Centre for Micro and Nano Engineering (CeMNE) College of Engineering, Universiti Tenaga Nasional (UNITEN) 43009 Kajang, Selangor, Malaysia.
[2]Institute of Microengineering and Nanoelectronics (IMEN) Universiti Kebangsaan Malaysia (UKM) 43600 Bangi, Selangor, Malaysia.

Abstract. This paper presents the modeling and optimization of 14nm gate length CMOS transistor which is down-scaled from previous 32nm gate length. High-k metal gate material was used in this research utilizing Hafnium Dioxide (HfO_2) as dielectric and Tungsten Silicide (WSi_2) and Titanium Silicide ($TiSi_2$) as a metal gate for NMOS and PMOS respectively. The devices are fabricated virtually using ATHENA module and characterized its performance evaluation via ATLAS module; both in Virtual Wafer Fabrication (VWF) of Silvaco TCAD Tools. The devices were then optimized through a process parameters variability using L9 Taguchi Method. There were four process parameter with two noise factor of different values were used to analyze the factor effect. The results show that the optimal value for both transistors are well within ITRS 2013 prediction where V_{TH} and I_{OFF} are 0.236737V and 6.995705nA/um for NMOS device and 0.248635 V and 5.26nA/um for PMOS device respectively.

1 Introduction

The gate length of MOSFET has continually been scaled down through last few decades to create smaller and smaller device in order to fabricate high density chips. Reduced power dissipation, faster switching and low cost were the main concern for this scaling. As MOSFET is scaled down it provides various kind of technical challenges and this become worsen when it comes to the nano-meter dimensions. This is because of the problems such as Short Channel Effects (SCE), increased leakage current, and lack of pinch off [1]. The utilization of SiO_2 to overcome the problems is no more effective today. Researchers has come up with a new solution to overcome the scaling impact by replacing the gate dielectric from SiO_2 to high permittivity materials and innovations to new device structure such as Finfet and double-gate. In this research, the virtual fabrication was simulated through ATHENA module and its electrical characteristic was simulated via ATLAS module where both modules can be found in Silvaco TCAD Tools. These modules are important in designing and optimizing the process parameter [2] of a semiconductor device. As part of

* Corresponding author: faizahz@uniten.edu.my

© The Authors, published by EDP Sciences. This is an open access article distributed under the terms of the Creative Commons Attribution License 4.0 (http://creativecommons.org/licenses/by/4.0/).

optimization process, Taguchi Method were used to observe the variance and mean effect of process parameter. With added noise factor called signal-to-noise ratio (SNR), this method becomes more reliable. The aim of this research is to virtually design and optimize a 14nm high-k metal gate CMOS transistor with threshold voltage, V_{TH} of 0.2301V and leakage current, I_{OFF} lower than 100nA/um. The values are set by ITRS 2013 specification.

2 Experiment description

2.1 Virtual transistor simulation recipes.

For simplicity, the transistors were designed separately in ATHENA module. The summarized simulation recipes were shown in Table 1. The complete virtual design of 14nm NMOS transistor is as shown in Fig. 1. The same structure was used to design the PMOS transistor except the utilization of metal gate which is Titanium Silicide ($TiSi_2$).

Table 1. Simulation Recipe

Process step	Parameters
Silicon substrate	• 7 x 10^{14} cm^{-3} Boron • <100> orientation
Retrograde well implantation	• 200Å oxide screen by 970˚C, 20 min of dry oxygen • 4.55 x 10^{11} cm^{-3} Phospor • 30 min, 900˚C diffused in nitrogen
STI isolation	• 130Å stress buffer by 900˚C, 25min of dry oxygen • 1500Å Si_3N_4, applying LPCVD • 1.0 um photoresist deposition • 15 min annealing at,900 ˚C
Gate oxide	Diffused dry oxygen for 0.1 min, 815 ˚C
Vt adjust implant	• 1.8 x 10^{11} cm^{-3} Boron difluoride • 5KeV implant energy, 7˚ tilt • 20 min annealing at, 795 ˚C
High-k metal gate deposition	• 0.002 um HfO_2 • 0.1 um WSi_2 (NMOS) • 0.1 um $TiSi_2$ (PMOS) • 17 min, 900 ˚C annealing
LDD implantation	• 7.553x 10^{13} cm^{-3} Phosphor (NMOS) • 5.05 x 10^{13} cm^{-3} Boron (PMOS) • 20˚ tilt
Sidewall spacer	• 0.047 um Si_3N_4
S/D implantation	• 0.99 x 10^{14} cm^{-3} Arsenic (NMOS) • 9.20 x 10^{12} cm^{-3} Boron (PMOS) • 10KeV implant energy, 7˚ tilt
PMD deposition	• 0.3 um BPSG • 25 min, 850 ˚C annealing
Metal 1	• 0.04 um Aluminium
IMD deposition	• 0.005 um BPSG • 15 min, 950 ˚C annealing
Metal 2	• 0.12 um Aluminium

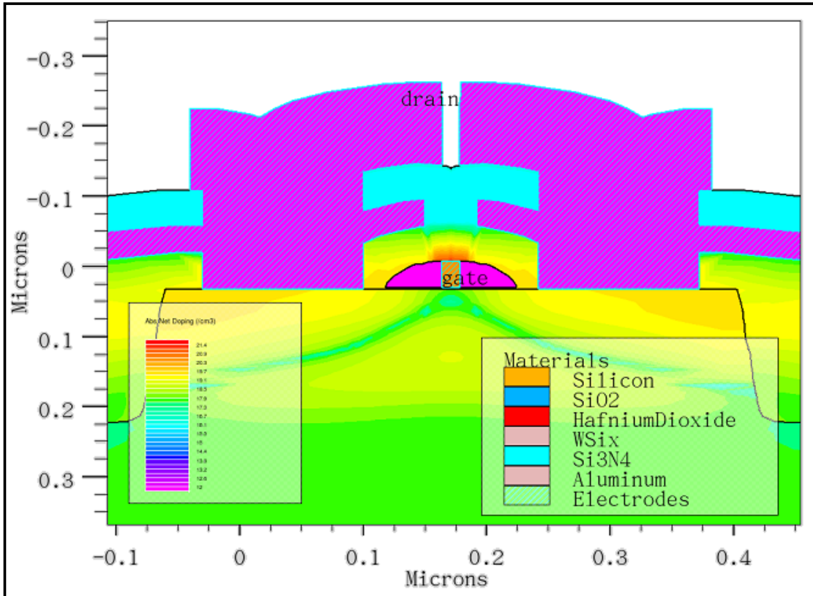

Fig. 1. Doping Profile of 14nm NMOS Transistor

2.2 Taguchi L9 orthogonal array method.

The optimization of the transistors was done using Taguchi Method by variation of the process parameters. The parameters that has been selected in this research includes Halo Implantation Dose (A), Halo Tilting Angle (B), Source Drain Implantation (C), and Compensation Implantation (D). Noise factors on the other hands includes Sacrificial Oxide Layer Temperature, BPSG Temperature and V_T Adjust Implant Temperature. Table 2 shows the value of each parameter at different level and Table 3 shows their noise factors for both type of device.

Table 2. Control Factors and Their Levels

Device	Symbol	Unit	Level 1	Level 2	Level 3
NMOS	A	atom/cm^3	7.5530x10^{13}	7.5535x10^{13}	7.5540x10^{13}
	B	°	31	32	33
	C	atom/cm^3	0.99x10^{14}	1x10^{14}	1.1x10^{14}
	D	atom/cm^3	0.67510^{14}	0.68x10^{14}	0.685x10^{14}
PMOS	A	atom/cm^3	5.05 x 10^{12}	5.10 x 10^{12}	5.15 x 10^{12}
	B	°	19.7	19.8	19.9
	C	atom/cm^3	9.00 x 10^{12}	9.10 x 10^{12}	9.20 x 10^{12}
	D	atom/cm^3	0.4 x 10^{11}	1.1 x 10^{11}	1.8 x 10^{11}

Table 3. Noise Factors and Their Levels

Device	Symbol	Noise Factor	Unit	Level 1	Level 2
NMOS	X	Sacrificial Oxide Layer Temperature	°C	900	910
	Y	BPSG Temperature	°C	850	852
PMOS	X	Sacrificial Oxide Layer Temperature	°C	900	910
	Y	Vt Adjust Implant Temperature	°C	795	800

3 Results and analysis

Taguchi method was applied in this research to optimize the threshold voltage (V_{TH}) and leakage current (I_{OFF}). By following the L9 Orthogonal Array template, all four control factors are varied accordingly using the dopant values for which produced the output near to the ITRS 2013 prediction. In this experiment V_{TH} belongs to nominal-the-best quality characteristic while I_{OFF} belongs to lower-the-best quality characteristic. The initial results of V_{TH} and I_{OFF} after optimization are described in Table 4 and Table 5 for NMOS transistor and PMOS transistor respectively.

Table 4. V_{TH} and I_{OFF} Results for NMOS

Exp No.	Threshold Voltage, V_{TH} (V)				Leakage Current, I_{OFF} (nA/um)			
	X1, Y1	X1, Y2	X2, Y1	X2, Y2	X1, Y1	X1, Y2	X2, Y1	X2, Y2
1	0.493733	0.485195	0.493934	0.485400	5.104570	5.650100	5.091970	5.636180
2	0.242297	0.230865	0.242553	0.231122	70.55158	78.12330	70.35110	77.94000
3	0.430243	0.438392	0.430030	0.438201	1599.700	16709.90	1597.930	1669.170
4	0.248580	0.239892	0.248834	0.240148	66.82820	72.31010	66.67090	72.14010
5	-0.169930	-0.169712	-0.169712	-0.178187	2029.080	2181.740	2025.230	2177.640
6	0.165606	0.156053	0.165873	0.156322	138.1950	149.9200	137.8750	149.5730
7	0.163056	0.171313	0.162839	0.171095	1912.970	2054.570	1909.310	2050.680
8	0.181527	0.172296	0.181792	0.172562	120.8040	131.0810	120.5230	130.5060
9	0.228356	0.219083	0.228613	0.219342	79.66340	86.54280	79.47660	86.34030

Table 5. V_{TH} and I_{OFF} Results for PMOS

Exp No.	Threshold Voltage, V_{TH} (V)				Leakage Current, I_{OFF} (nA/um)			
	X1, Y1	X1, Y2	X2, Y1	X2, Y2	X1, Y1	X1, Y2	X2, Y1	X2, Y2
1	0.24358	0.243365	0.24315	0.242937	52.217	52.422	52.6363	52.8428
2	0.237851	0.237633	0.237386	0.237168	58.3183	58.5485	58.8322	59.0647
3	0.231531	0.231313	0.23103	0.230812	65.9534	66.2154	66.5826	66.8475
4	0.250575	0.250366	0.250189	0.249976	45.2084	45.3838	45.5318	45.7087
5	0.233934	0.233719	0.233523	0.23331	65.0706	65.324	65.5665	65.8223
6	0.262981	0.26277	0.262545	0.262332	35.6784	35.818	35.9749	36.1159
7	0.244912	0.2447	0.244515	0.244302	52.3622	52.5649	52.7469	52.9514
8	0.274721	0.274513	0.274348	0.274136	52.217	52.422	52.6363	52.8428
9	0.258453	0.258243	0.258061	0.257852	58.3183	58.5485	58.8322	59.0647

The next step is to determine the dominant and the adjustment factor for both transistors. The results were summarized in Table 6 for both V_{TH} and I_{OFF}. For NMOS device, it can be seen that Halo Implantation (**A**) shows the highest influence on V_{TH} (40%) and hence it was set to be the dominant factor. Halo tilting angle (**B**) on the other hand displays the lowest impact of 13% on variance but score the highest on Mean (29%). Thus, parameter **B** was set to be the adjustment factor. Parameter **B** was then varied between 31° to 33° to get the V_{TH} value near to ITRS 2013 prediction. For I_{OFF}, S/D Implantation (**C**) gives the highest impact (79%) to the device and thus it was set as a dominant factor.

The S/N response for PMOS device shows parameter **A** as the dominant factor because of the highest influence on V_{TH} (52%) and parameter **B** as the adjustment factor due to highest score on mean (56.23%) and lowest score on variance (32%). Parameter **C** and **D** was neglected and considered null as the percentage scores below 10%. It is because any changes made to parameter **C** and **D** will not influences the device performance. Parameter **B** was swept between 19.7° to 19.9° to get the V_{TH} within the ITRS 2013 prediction. The same response for I_{OFF} as parameter **A** possess the highest value on Mean (46%) and thus was set to be the dominant factor.

Table 6. S/N Response and Annova

Device	Process Parameter	V_{TH}					I_{OFF}			
		S/N Ratio (dB)			Factor Effect (%)		S/N Ratio (dB)			Factor Effect (%)
		L1	L2	L3	Variance	Mean	L1	L2	L3	Variance
NMOS	A	29.9	21.6	29.7	40	46.00	137.6	131.2	131.2	1
	B	24.6	30.0	26.6	13	29.00	140.9	131.4	124.7	11
	C	29.6	29.4	22.1	32	18.00	146.7	142.5	107.8	79
	D	30.4	25.0	25.7	15	7.00	140.2	131.2	125.5	9
PMOS	A	56.7	57.6	58.1	52	56.23	56.7	57.6	58.1	46
	B	58.0	57.5	57.0	32	40.56	58.0	57.5	57.0	14
	C	57.3	57.5	57.7	4	3.01	57.3	57.5	57.7	38
	D	57.1	57.5	57.8	12	0.19	57.1	57.5	57.8	2

The best setting parameters for both devices based on the Taguchi analysis are shown in Table 7. The best setting of parameter values was simulated again at different noise factor to verify the accuracy of Taguchi analysis. The result of the confirmation experiment based on different noise factors are shown in Table 8. Final results were then compared to ITRS 2013 prediction for conclusion of the optimization process experiment which is shown in Table 9.

Table 7. S/N Response and Annova

Device	Process Parameter	Unit	Best Value	
			V_{TH}	I_{OFF}
NMOS	A	atom/cm^3	7.5530x10^{13}	7.5530x10^{13}
	B	°	32	31
	C	atom/cm^3	0.99x10^{14}	0.99x10^{14}
	D	atom/cm^3	0.675x10^{14}	0.675x10^{14}
PMOS	A	atom/cm^3	5.15 x 10^{12}	5.15 x 10^{12}
	B	°	19.7	19.7
	C	atom/cm^3	9.20 x 10^{12}	9.20 x 10^{12}
	D	atom/cm^3	1.8 x 10^{11}	1.1 x 10^{11}

Table 8. Results of Confirmation Experiment

Device	Performance Parameter	X1, Y1	X1, Y1	X1, Y1	X1, Y1	Average Value
NMOS	V_{TH} (V)	0.242397	0.230766	0.242653	0.231132	0.236737
	I_{OFF} (nA/um)	6.704570	7.150100	6.891970	7.236180	6.995705
PMOS	V_{TH} (V)	0.24892	0.24873	0.24856	0.24833	0.24864
	I_{OFF} (nA/um)	5.23622	5.25649	5.27469	5.29514	5.26564

Table 9. ITRS Prediction vs. Optimization Results

Device	Performance Parameter	ITRS Prediction	Optimization Results
NMOS	V_{TH} (V)	0.23	0.236737
	I_{OFF} (nA/um)	<100	6.995705
PMOS	V_{TH} (V)	0.230	0.248635
	I_{OFF} (nA/um)	<100	5.258260

4 Conclusion

The modeling and optimization of 14nm gate length high-k metal gate CMOS transistor was successfully presented. The optimization of threshold voltage (V_{TH}) and leakage current (I_{OFF}) through Taguchi analysis was also fully utilized together with Silvaco TCAD Tools for virtual design simulations. The results were reported to be well within ITRS 2013 prediction.

We would like to thank Universiti Tenaga Nasional (UNITEN) and the Malaysian Ministry of Education for sponsoring the publication of this work using grant 20140123FRGS.

References

1. F. Matsuoka, H. Iwai, H. Hayashida, K. Hama, Y. Toyoshima, K. Maeguchi, *IEEE Trans. Electron Devices*, **37(6)**, 1487 (1990)
2. K. Goel Ashok, M. Merry, K. Arkenberg, E. Therkildsen, E. Chiaburu, W. Standfest, Silvaco International, (1995)
3. Z.N. Faizah, I. Ahmad, P.J. Ker, P.A. Roslan, A.A. Maheran. *IEEE Regional Symposium*, 1 (2015)
4. H.A. Elgomati, B.Y. Majlis, A.A. Hamid, P.M. Susthitha, I. Ahmad, *Sixth Asia Modelling Symposium*, 40 (2012)
5. A.A. Maheran, P.S. Menon, I. Ahmad, H.A. Elgomati, B.Y. Majlis, F. Salehuddin, 10th *IEEE International Conference*, 173 (2012)
6. I. Ahmad, Y.K. Ho, B.Y. Majlis, Quantum Electronics & Optoelectronics, **9(2)**, 40 (2006)