Process Characterization of 32nm Semi Analytical Bilayer Graphene-based MOSFET

Z.A. Noor Faizah[1,*], *Ibrahim* Ahmad[1] , *P.J.* Ker[1] , and *P.S.* Menon[2]

[1]Centre for Micro and Nano Engineering (CeMNE) College of Engineering, Universiti Tenaga Nasional (UNITEN) 43009 Kajang, Selangor, Malaysia
[2]Institute of Microengineering and Nanoelectronics (IMEN) Universiti Kebangsaan Malaysia (UKM) 43600 Bangi, Selangor, Malaysia

Abstract. This paper presents an inclusive study and analysis of graphene-based MOSFET device at 32nm gate length. The analysis was based on top-gated structure which utilized Hafnium Dioxide (HfO_2) dielectrics and metal gate. The same conventional process flows of a transistor were applied except the deposition of bilayer graphene as a channel. The analytical expression of the channel potential includes all relevant physics of bilayer graphene and by assuming that this device displays an ideal ohmic contact and functioned at a ballistic transport. Based on the designed transistor, the on-state current (I_{ON}) for both GNMOS and GPMOS shows a promising performance where the value is 982.857uA/um and 99.501uA/um respectively. The devices also possess a very small leakage current (I_{OFF}) of 0.289578nA/um for GNMOS and 0.130034nA/um for GPMOS as compared to the conventional SiO_2/Poly-Si and high-k metal gate transistors. However, the devices suffer an inappropriate subthreshold swing (SS) and high value of drain induced barrier lowering (DIBL).

1 Introduction

The never ending process challenge of scaling down to cramming more transistor in a single chip which was coined by Gordon E. Moore has led to an invention of new device design and proposed materials. Problems such as transport degradation, the increasing of parasitic effect and aggravated on-off transition attributed from the miniaturization of the channel length. From conventional SiO_2/Poly-Si to high-k metal gate, advanced silicide and multi-gate transistors; all has been adopted to overcome the problems. Further ahead, the carbon-based material is proposed as an alternative to SiO_2 and now is rising in nano-electronic design due to low cost of manufacturing and its outstanding properties such as extremely high mobility together with a promising ability to be scaled down to a smaller gate length. The development of Carbon Nanotubes (CNT) transistor is first introduced but due to significant gap in nanoribbons which can only be obtained at widths close to 1-2 nm [1] makes the CNT prohibited for fabrication on the scale of integrated circuit. Graphene was then introduced theoretically and experimentally [1-5]. The outcome shows that

* Corresponding author: faizahz@uniten.edu.my

graphene demonstrated to be thermodynamically stable and the 2-D nature of graphene has been confirmed by experimental observation of the quantum hall effect.

In addition, the fact that graphene is a planar form draws a major advantage over CNT, which mostly permits for highly developed top-down CMOS-compatible process flow [6]. In this research, a 32nm gate length of NMOS and PMOS bilayer graphene-based transistor were virtually design and tested for its functionality where the performance parameters were set to be in line with the International Technology Roadmap of Semiconductor, ITRS 2011 prediction for which the threshold voltage (V_{TH}) is 0.103 ± 12.7% V, on-state current (I_{ON}) greater than 100nA/um and leakage current (I_{OFF}) lower than 150nA/um. The simulation tools of ATHENA and ATLAS in Silvaco TCAD Tools was utilized during the simulation process.

2 Transistor virtual fabrication for simulations

In this experiment, both GNMOS and GPMOS transistor are virtually fabricated and analyzed separately. This is to simplify the simulation process and comparison of the device performance. The fabrication processes for both devices were similar except the types the dopant use; which is differs at its substrate, and its density of dopant. A single crystal of silicon wafer (100) with a heavily doping concentration was initially prepared. It was then thermally oxidized to a SiO_2 layer to create a p- and n-wells for NMOS and PMOS transistor. Graphene is then atomically deposited onto the SiO_2 layer where the thickness and the number of vertical grid spacing are practically specified according to the established simulation and fabrication results [2, 6-9].

Next, a thickness of 0.67 nm high-k material, Hafnium Dioxide (HfO_2) is then deposited onto graphene layers followed by 38nm thickness of different metal gate for GNMOS and GPMOS transistor. The metal gate that is used for GNMOS and GPMOS transistor is Tungsten Silicide (WSi_2) and Titanium Silicide ($TiSi_2$) respectively. The high-k and metal gate materials are etched precisely to produce a gate length of 32 nm (± 0.1nm) transistor. Then, Halo and Source-Drain (S/D) structures using heavily doped n-type and p-type material are implant to accumulate the Schottky tunneling source and drain. The function is to provide a low resistive path for only electrons or holes to be inoculated into the graphene channel and thus achieved a unipolar conduction. Compensation implantation of Phosphor dopant at 10^{12} cm^{-3} took place right after the growth of 0.015um Borophosphosilicate Glass (BPSG). Aluminum layer is then deposited to form the metal contact of the transistor which also dictates that the process is accomplished and ready for performance measurement through its electrical characterization. The complete design of 32 nm planar NMOS bilayer graphene transistor is as shown in Fig. 1.

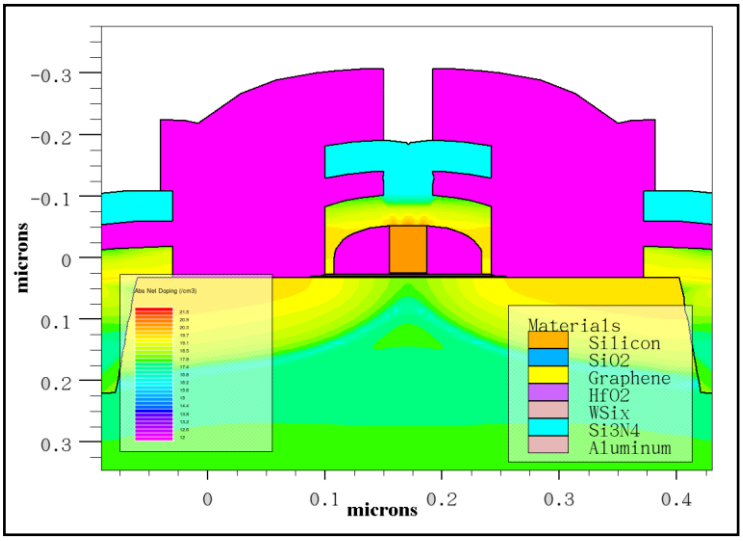

Fig. 1. Doping Profile of 32nm NMOS Bilayer Graphene Transistor

3 Physical characterization of graphene transistor

The complete design of virtual transistors was then ready for their electrical characterization using ATLAS simulator. At this stage, the performance of the transistors was measured in terms of threshold voltage (V_{TH}), leakage current (I_{OFF}), and on-state current (I_{ON}) which was specified in International Technology Roadmap of Semiconductor (ITRS) 2011. In this research, bilayer graphene was modeled as a semi-metal with a bandgap of approximately 0.55eV [3], permittivity of 2.4 [6], charge carrier mobility of top-gated graphene measured at room temperature and effective field of Eeff=0.4MV/cm [6]. The radiative recombination rate of electron and holes in graphene is set at 100ns [9]. The graphene's 2-Dimensional (2D) electron and hole densities of states are measured at 300K and obtained from equations below [9]:

$$Nc = \frac{8\pi m_e kT}{h^2}\ln\left(1 + e^{-(Ec-Ef)/kT}\right)$$
$$Nv = \frac{8\pi m_h kT}{h^2}\ln\left(1 + e^{-(Ef-Ev)/kT}\right) \quad (1)$$

where the effective masses of electrons and holes in graphene in this research was set at me ≈0.06 mo and mh≈0.03mo while mo is the free electron mass according to paper in [8]. This is due to the transport properties of graphene attributed to a single spatially quantized sub band which is populated by electrons and holes at that value. The number of electrons and holes per unit area are experimentally measured to be ~10^{12}cm^{-2} at room temperature which also satisfies (1) [9].

4 Results and analysis

The electrical characteristic curves of a graphene transistor with a heavily doped n- and p-type Silicon S/D were shown in Fig. 2 and Fig. 3. Fig. 2 shows the I_{DS}-V_{GT} characteristics of GNMOS at different V_{DS} and Fig. 3 shows the I_{DS}-V_{GT} characteristics of GPMOS at different V_{DS}. The device's performance is measured at fixed threshold voltage, V_{TH} = 0.103 V ± 12.7% as guided by ITRS 2011 by variating the dopant density and annealing temperature. From, ITRS 2011 prediction, the on-state current (I_{ON}) is aimed to be greater than 100nA/um and leakage current (I_{OFF}) lower than 150nA/um.

In this experiment, the I_{ON} of graphene-based transistor was closer to the ITRS 2011 prediction and slightly higher than conventional SiO_2/Poly-Si [10] and high-k metal gate [11, 12] transistors due to low effective mass and less energy required to go through the outlawed gap between source and drain [3]. Leakage current (I_{OFF}) of graphene-based transistor possess a good value not only lower than the conventional SiO_2/Poly-Si and high-k metal gate transistor but so much lower than the ITRS 2011 prediction. The high value of I_{ON} and lower value of I_{OFF} will boost up the switching capability of a transistor which was proven in this simulation, $I_{ON}/I_{OFF} \approx 10^6$. However, due to the minority carrier (hole) concentration in graphene was very high, this device suffers a large subthreshold swing (SS) and drain-induced barrier lowering (DIBL) [9]. The performance results for both GNMOS and GPMOS were summarized in Table 1.

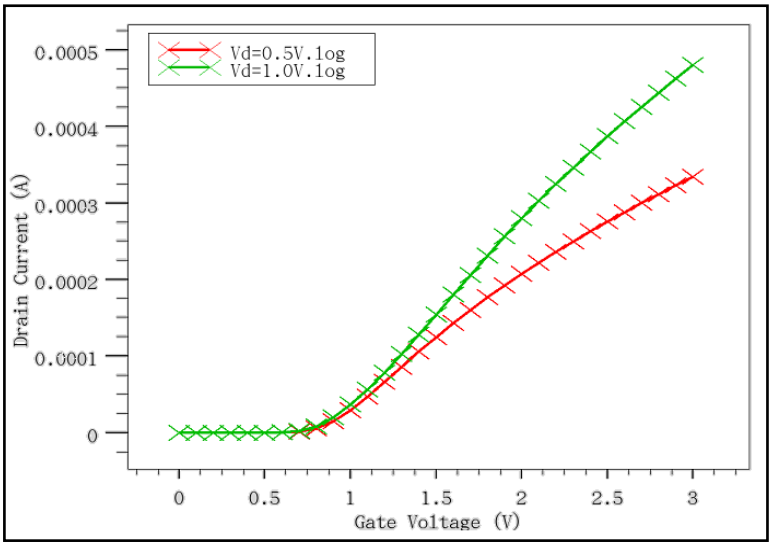

Fig. 2. I_{DS}-V_{GT} of GNMOS at different V_{DS}

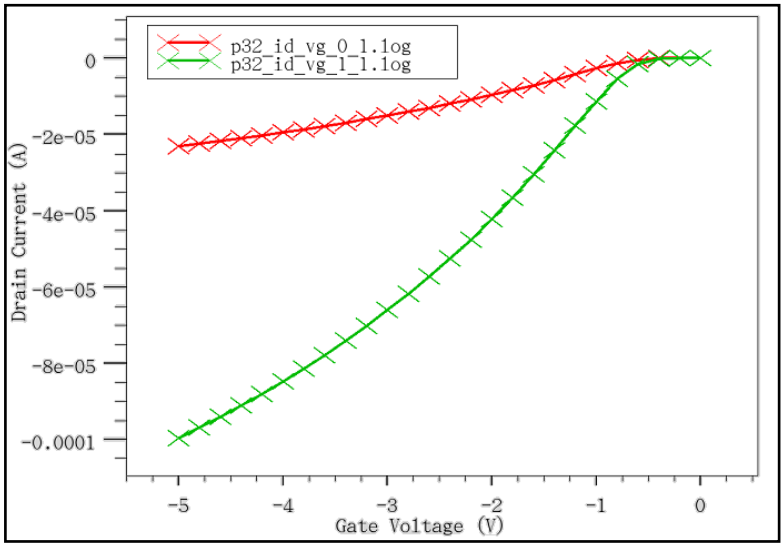

Fig. 3. I_{DS}-V_{GT} of GPMOS at different V_{DS}

Table 1. Performance Analysis of 32nm Graphene-based Transistor

Parameter	GNMOS	GPMOS
High-K/Metal Gate	HfO_2/WSi_2	$HfO_2/TiSi_2$
Threshold Voltage, V_{TH} (V)	0.103444	0.103184
On-state current, I_{ON} (uA/um)	982.857	99.501
Leakage current, I_{OFF} (nA/um)	0.289578	0.130034
Sub-threshold Swing, SS (mV/dec)	94.38	119.92
Drain-Induce Barrier Lowering, DIBL (mV/V)	134.6	30.112
On-Off ratio (I_{ON}/I_{OFF})	3.394×10^6	0.765×10^6

5 Conclusion

The performance of 32nm gate length of planar graphene-based transistor were analyzed in the paper. The utilization of highly-doped Silicon S/D which forms a Schottky tunneling junction resulted in high I_{ON} while the application of top-gated high-k metal gate material modulates the drain current and limits the carrier mobility. The results show a very high I_{ON} with such a low value of I_{OFF}. This confirms that the utilization of graphene layer is possible to be implemented with an obligatory to enhance the device performance by bandgap tuning method.

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