Area-efficient readout with 14-bit SAR-ADC for CMOS image sensors

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Abstract. This paper proposes a readout design for CMOS image sensors. It has been squeezed into a 7.5um pitch under a 0.28um 1P3M technology. The ADC performs one 14-bit conversion in only 1.5us and targets a theoretical DNL feature about +1.3/-1 at 14-bit accuracy. Correlated Double Sampling (CDS) is performed both in the analog and digital domains to preserve the image quality.
Keywords— CMOS Image Sensor, Successive-Approximation-Register ADC, Column-parallel architecture, CDS

1 Introduction

Recently introduced CMOS image sensors (CIS) have been following an evolutionary trend in the last years. One benchmark for this is the dramatic growth of patents mainly for process [1]. This technological breakthrough yields an added value along with new design solutions.

Applications like automotive, surveillance and broadcast cameras require high quality moving pictures in terms of speed, accuracy and compactness. This represents a good opportunity to exploit the process progress. Still mode for Digital Still Cameras (DSC) for instance is also an important development area were resolution can be justified until 14 or 16 bit.

Column-parallel readout is commonly used for a high frame rate and low power operation. Four main architectures can be distinguished for the Analog to Digital Converter (ADC) cells. : the Single Slope ADC (SS-ADC), the Successive-Approximation-Register ADC (SAR-ADC) [2-3], the Cyclic ADC (CY-ADC) and the Delta-Sigma ADC (ΔΣ-ADC). The SS-ADC is mainly bound by the clock high frequency required for high speed and high resolution applications. The CY-ADC suffers from high power consumption as the bit resolution increases due the open-loop gain requirements of the amplifier. ΔΣ-ADCs present intrinsic good noise performances coming with the noise shaping but they suffer from low speed operation and require also additional digital filters.

In this paper, a new architecture of column-parallel SAR-ADC adapted for CMOS image sensors is presented. Conversion time has been optimized to reach 1.5us over 14-bit resolution. In [3], a 14-bit SAR-ADC has been reported with a layout pitch of 11.2um as shown in Table1. In [2] ADC pitch reached 8.4um. In this work, the design has been squeezed into 7.5um pitch. The adopted solutions are also easily adaptable to a 12-bit 5.6um ADC pitch making it compatible with next generation automotive sensors.

In each column of the imager, a Programmable Gain Amplifier (PGA) is implemented just before the SAR-ADC to ensure different analog gains. Such an operation relaxes the constraints on the ADC input-referred noise. During our discussion, the PGA plus the SAR-ADC are called the readout.

The layout has been implemented both under Front Side Illumination (FSI) and Back Side Illumination (BSI) in a 1P3M 0.28um process. Another flexibility advantage of the design is the high voltage swing. It has been validated for 1V5 voltage swing and can be extended to 1V7 making it compatible with next generation pixels.

Table 1. State of art of 14-bit SAR-ADCs.

Ref.	ADC Type	Resolution	ADC Pitch (um)	Conversion Time (us)
[2]	SAR	14	8.4	1.7
[3]	SAR	14	11.2	-
This Work	SAR	14	7.5	1.5

In this paper, we will present in Section 2 the architecture of the image sensor with emphasis on the readout operation. Section 3 details a novel scheme 14-bit SAR-ADC architecture and design considerations. Section 4 gives an overview of layout solutions.

2 Image sensor architecture

2.1 Bloc diagram

The modular architecture of the image sensor is depicted in Figure 1(a). The present work consists on designing the pre-amplification and the SAR-ADC.

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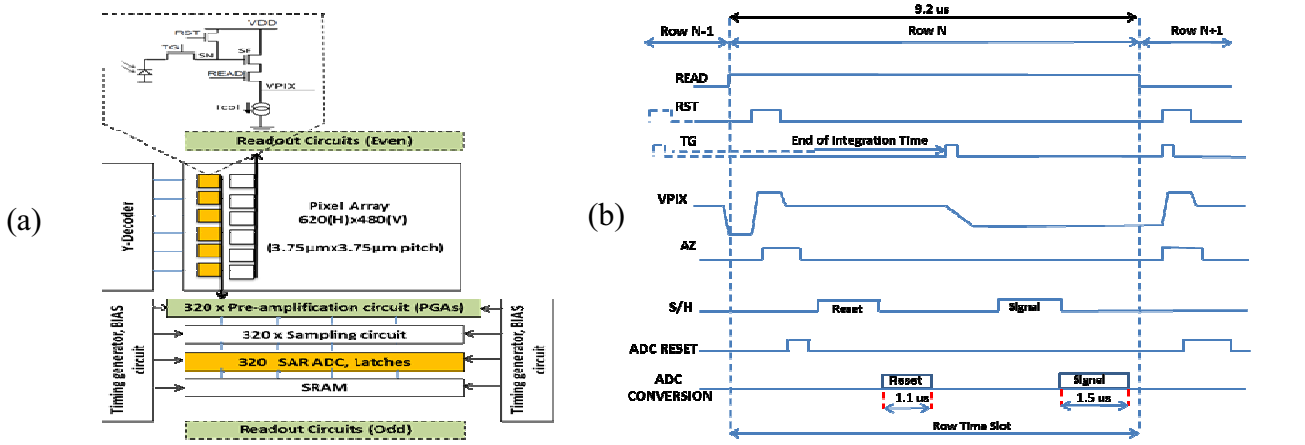

Figure 1. Image Sensor (a) Overall Architecture (b) Readout Operation

A Static Random Access Memory (SRAM) bloc is implemented to save data prior to the transfer out to a Field Programmable Gate Array (FPGA) for processing. The active pixel sensor array is based on a 4-transistor type pinned photo diode (PD) and is driven by a vertical driver (Y-Decoder). Signal RST for resetting, TG for charge transfer and READ for pixel reading can be set by the Y-Decoder. The pixel pitch is 3.75um. A top and bottom readout disposition is adopted so as to benefit from a double pitch layout.

2.2 Readout operation

The readout timing analysis is shown in Figure 1(b). A 9.2us line period has been reached. It includes the pixel, the PGA and the ADC operations.

A first TG pulse allows dumping out residual charges from the photodiode. The second one ensures charges transfer to the Sensing Node (SN) presented by the gate of the source follower (SF) shown in Figure 2. The PGA is first initialized by means of an auto-zero (AZ) signal. Various analog gains 2^0 .. 2^4 are ensured by the PGA by selecting binary weighed feed-back capacitors (CFB). The PGA output is sampled (S/H) prior to each ADC conversion. Two ADC conversions are performed: one for the reset and one for the signal so as to do a digital Correlated Double Sampling (CDS) operation. The reset conversion is performed over only 10-bit during 1.1us in order to save power.

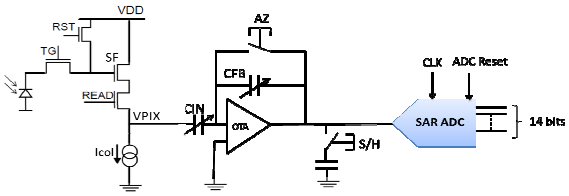

Figure 2. Simplified Schematic of the Pixel and the Readout

3 Compact 14-bit SAR-ADC

3.1 ADC architecture

The SAR-ADC consists of a Digital-to-Analog converter (DAC) and a multistage comparator (Preamp1, Preamp2 and a Latch) as shown in Figure 3(a). The preamplifiers preamp1 and preamp2 ensure the analog gain and mitigate the kick-back noise due to the Latch. The DAC consists of a charge distribution-based capacitor array.

This SAR architecture is developed to be suitable with imager's context where specific features should be taken into account namely:

- Compactness for 7.5um pitch design
- Low power operation to limit the dark current
- Common control of all ADCs
- Image quality considerations: Uniformity of ADCs across the imager, immunity to crosstalk, horizontal (X) and vertical (Y) droop effects, offsets and noise, dispersions, …

Compactness within 7.5um pitch has been ensured through a specific use of multiple reference voltages as depicted in Figure 3(a). This technique allowed reaching 14-bit resolution with only 7 binary weights 2^0 … 2^6. Two additional fractional references Vfractional1 and Vfractional2 are used in addition to the primary ones Vref0 and Vref1 that define the Dynamic Range (DR) of the ADC according to (1). Theses reference voltages are correlated as follows:

$$DR = Vref1 - Vref0 \tag{1}$$

$$Vref0 = 0V \qquad Vref1 = 1.5V \tag{2}$$

$$Vfractional0 = \frac{Vref1 - Vref0}{2^7} = \frac{DR}{2^7} \approx 11.71mV \tag{3}$$

$$Vfractional1 = Vref1 + \frac{Vref1 - Vref0}{2^7} \approx 1.5V + 11.71mV \tag{4}$$

ADC operation timing analysis is shown in Figure 3 (b) in the case of six bit conversion for simplicity. The 14-bit SAR conversion consists of two steps of classical SAR conversions of 7-bit resolution each. The first step extracts the seven Most Significant Bit (MSB). It is performed between the primary references Vref1 and Vref0. The second step is performed using Vfractional1 and Vfractional0 to extract the seven Least Significant Bit (LSB). An extra clock cycle is required between these two steps to ease the transition by means of Multi-Vrefs devices controlled by a common control signal. The final binary 14-bit word is obtained following a concatenation of both 7-bit words. Dynamic power consumption is optimized by a straight-forward SAR operation as depicted in Figure 3(c).

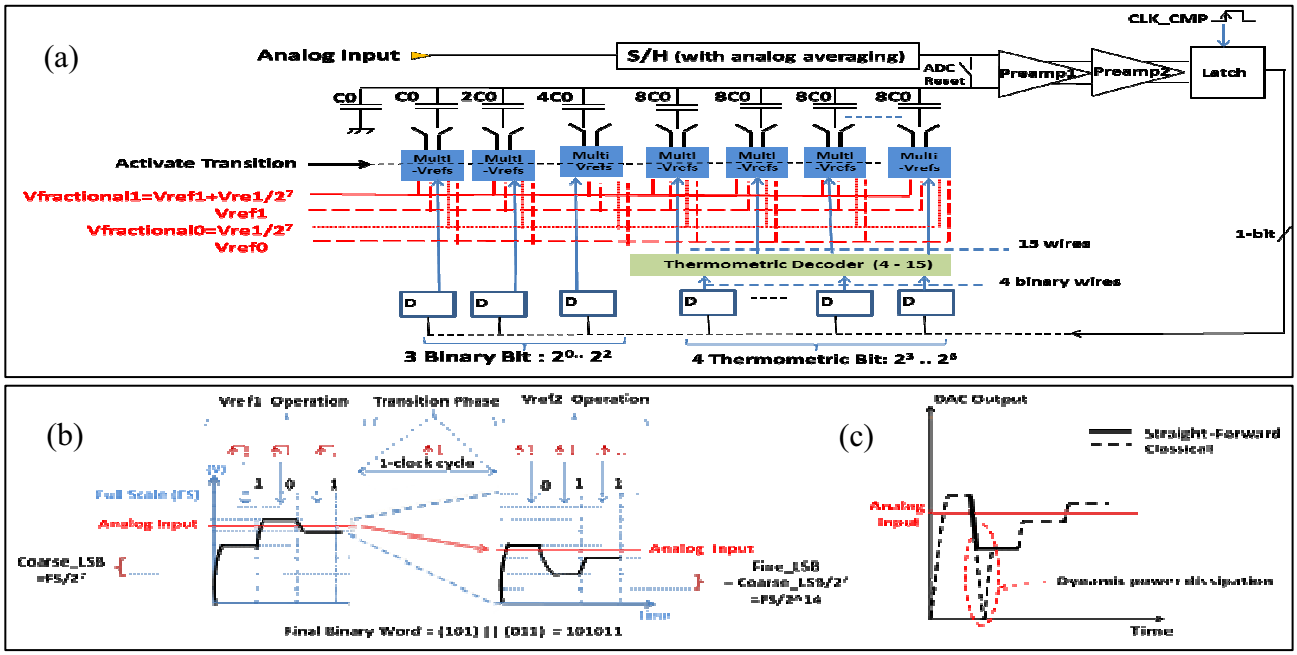

Figure 3. Novel scheme 14bit SAR-ADC(a) Architecture(b) ADC Operation for 6bit conversion(c) Straight-forwad switching scheme

3.2 Linearity analysis

Two main error contributors can be identified for the linearity issues: The DC accuracy of the reference voltages and the capacitors mismatching due to the fabrication process. In fact, the fractional reference voltages Vfractional1 and Vfractional0 have to be matched up to a 14-bit resolution with regard to the main references Vref1 and Vref0. According to (5) and (6), the module of δ1 and δ0 have to remain below one LSB given by (7). A calibration algorithm has been defined to correct for this issue and is beyond the scope of this paper.

$$Vfractional0 = Vfractional0\_Nom + \delta_0 \tag{5}$$

$$Vfractional1 = Vfractional1\_Nom + \delta_1 \tag{6}$$

$$LSB = \frac{Vref1 - Vref0}{2^N} = \frac{1.5V}{2^{14}} \approx 91uV \tag{7}$$

To illustrate this effect, a behavioral simulation of the ADC has been performed over the dynamic range with the parameters indicated in Figure 4(a). Comparatively, the fractional references induced Differential-Non-Linearity (DNL) error is given by (8).

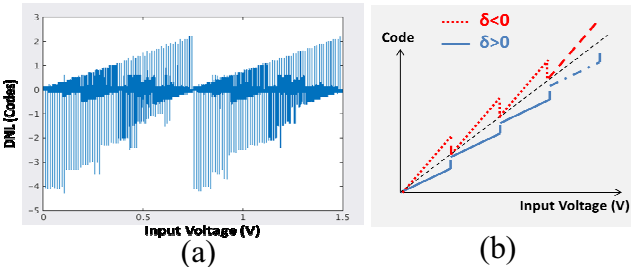

Figure 4. DNL errors due to fractional reference voltages shift: (a) δ0= - 4LSB, δ1= +2LSB (b) Impact on transfer characteristic

To explain, any shift δ on either fractional references will result into a slope variation between the coarse and the fine operations as depicted in Figure 4(b).

At a unity gain ADC transfer characteristic if neglecting attenuations, one LSB error on the input voltage axis results into one code DNL error.

$$DNL\_error = \frac{\delta}{LSB} \tag{8}$$

Simultaneously, the capacitors dispersion affects the DNL where the process matching is generally limited to 10-bit. Based on matching figures from a similar technology, the proposed architecture has been simulated in a fully binary DAC configuration. The results are shown in Figure 5(a). Capacitors were assumed to have a mean value and an error term according to:

$$C = C_{No\min al} + \delta_{err} \tag{9}$$

With δerr assumed to be Independent Identically Distributed (i.i.d) binary weighed Gaussian Random Variables. Clearly, the simulations confirm the presence of missing codes and decision levels. For this purpose, thermometric decoding has been applied to the four MSB as shown in Figure 3(a). This choice is based on a trade-off between the layout feasibility and DNL performances. Final DNL simulation results are shown in Figure 5(b) where +1.3 /-1 features is obtained at a 14-bit accuracy.

Integral-Non Linearity (INL) is less critical in the imaging context since we are mainly bound by the linearity of the pixel ~1%. The proposed architecture with thermometric decoding reaches an INL feature about +5.3/-9 at a 14-bit accuracy. Such a result guarantees 1‰ of linearity which is ten times better than that of the pixel.

Constant gain dispersion between columns, however, could cause important image artefacts. In this work, the Photo Response Non-Uniformity (PRNU) has been considered as a reference. It characterizes the inherent gain mismatch between the pixels and is about 5‰. Consequently, we targeted 0.5‰ (11-bit) of gain dispersion across the imager for the readout including the PGA and the ADC.

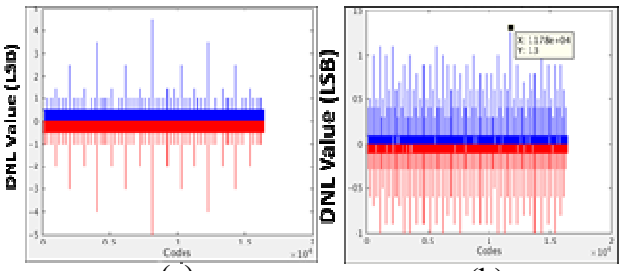

Figure 5. DNL results of the proposed SAR architecture: (a) Binary DAC (b) With thermometric decoding

4 Layout considerations

A prototype of 336 parallel readouts has been implemented respecting the 7.5um pitch. It is important to realize that the capacitor array is the most critical part especially in such a massive parallelism context. The array consists of 128 identical capacitive elements to ensure matching and thus DNL performances. This corresponds to 2^7xC0 of total DAC capacitance as already shown in Figure 3(a). Association between these elementary capacitors is made to form 2xC0, 4xC0 and 15 thermometric elements of value 8xC0. This association is made in a stamped way to further improve matching. The total length of the capacitor array is about 600um. To mitigate the gradient effect, thermometric 8xC0 elements are ordered one next to the other in the same order of the thermometric wires. In other words, it is only needed to ensure matching between two subsequent elements to preserve DNL.

With the Signal to Noise Ratio (SNR) and crosstalk in mind, plate capacitor technology has been adopted as shown in Figure 6(a). The idea consists on protecting the comparator input node from attenuation and noise. Metal2 has been chosen to route this node which benefits from low parasitic capacitance with respect to the ground. Post Layout Simulations (PLS) results show a DR of the ADC of 1.370V and a clipping at the end of the transfer characteristic due to attenuations as shown in Figure 6(b). Introducing the resulting DR in (7) gives (10). The SNR is then only decreased by 0.7dB compared to the initial LSB according to (11). ADC layout length reaches 1250um in a 7.5um pitch (Cf.Figure 6(c)).

$$LSB = \frac{1.370V}{2^{14}} \approx 84uV \tag{10}$$

$$SNR\_Loss = 20 * \log_{10} \frac{84}{91} \approx -0.7dB \tag{11}$$

Capacitors bottom plates, conveying reference voltages, are used as metal shielding as depicted in Figure7. The crosstalk worst case occurs when one column ADC converts zero signal whereas a maximum one is being converted by the two adjacent ADCs. PLS shown in Table2 indicate one code error on the middle column due to leakage problems during the 9.2us line timing which proves immunity to crosstalk.

Table 2. Output codes of PLS of three adjacent ADCs

ADC	Left ADC (Vin=1V5)	Middle ADC (Vin=0V)	Right ADC (Vin=1V5)
Output Code	11..111	00..001	11..111

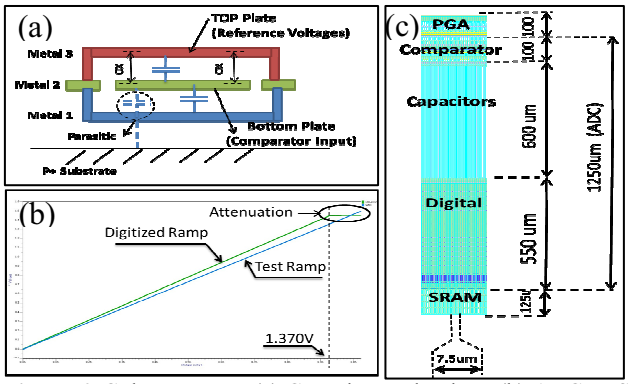

Figure 6. Column Layout(a) Capacitor technology (b) ADC PLS simulation of the transfer characteristic (c) 16 Columns layout

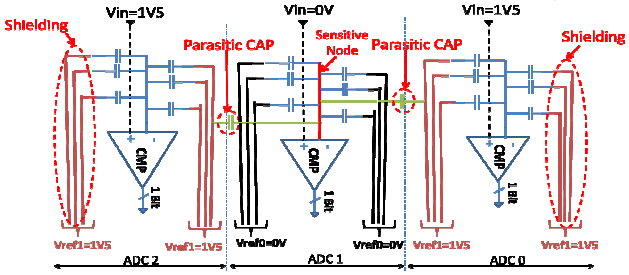

Figure 7. Worst case crosstalk and mitigation by metal shielding

5 Conclusion

In this work, a novel scheme SAR-ADC design for CMOS image sensors is proposed. It targets a DNL feature of +1.3/-1 over 14-bit. Our previous work [4] reported a DNL of +0.9/-0.7. This is due to trade-offs made in the layout phase. Final results will depend on the measurements of the prototype.

Future researches will be focused towards reference voltages. In addition to DC accuracy requirements mentioned above, drive capability remains a challenge to overcome mainly for a large columns number where steep current flows are needed. For the implemented 336 columns prototype, large reservoir capacitors have been used in addition to external reference voltages.

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