

A Study on High Density Gate-Oxide Anti-Fuse PROM Memory Cell Program Features

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Abstract. The program consistency of high density gate-oxide anti-fuse PROM (programmable read only memory) memory cell is considered in this paper. To solve this problem, we do research on the mechanism and models of gate-oxide break down. A test chip based on 2T memory cell is also designed for the experiment. During the test, we have found that the program consistency of 2T cell is really pessimistic. What's more, the program voltage has effect on the consistency. Through research and test, we have got the optimal program voltage-6.5V for 2T memory cell in 180nm technology. To further improve the consistency, we modify the 2T memory cell and propose a 3T memory cell. It consumes 18% more area, but the standard deviation of equivalent resistance decreases 15.3% in the worst situation. The deviation can decrease 80.3% at most. The program consistency is greatly improved.

1 Introduction

Anti fuse is a very significant kind of programmable interconnected cell. The semiconductor device based on anti fuse has very advanced performance in the following aspects(1)Non volatile cell(2)radiation hardened cell (3)high reliability (4) confidentiality(5)100% testability (6)small area, high velocity and low power consumption [1]-[3].

At present, the most typical and mature anti fuses are ONO (Oxide-Nitride-Oxide) type, α -Si (Amorphous Silicon) type and gate oxide type. Compared with ONO and α -Si anti fuse, gate oxide anti fuse has its particular advantage: it is entirely compatible with the standard CMOS technology. This advantage makes the cost decreased greatly. The design procedure also becomes more convenient.

PROM is a kind of high reliable device which is applied in many important fields. It has cruel requirements on the memory cell's performance and reliability. Conventional PROM uses e-fuse memory cell. E-fuse memory cell may get together again after the cell is has been fused. The cell which is not programmed may also be fused due to high current during the read motion. These problems make poor reliability of e-fuse PROM.

Gate-oxide anti fuse is a good choice for PROM memory cell. Compared with e-fuse memory cell, gate-oxide anti fuse memory cell improves a lot in reliability, anti-radiation performance and confidentiality. Gate-oxide anti fuse's performance corresponds to the ONO type's and α -Si type's and it can cut the cost greatly.

Gate-oxide anti-fuse memory cell also has a very typical defect. That is the poor consistency of the programmed cell. The equivalent resistance of memory

cell distribute from several hundred ohms to several hundred kilo ohms. The mega ohms situation exists, too. This defect increase the difficulties in designing the sense amplifier. The read speed of PROM is also facing a big challenge. If the equivalent resistance is too large, the circuit may even fail. The program consistency of gate-oxide anti fuse memory cell is awaiting for improve right now.

In this paper, we study on the mechanism and model of gate oxide break down and design test chips for experiment. The 2T memory cell's program consistency is carefully studied. We have also built a model for the programmed memory cell equivalent resistance. With this model, we assess the program consistency, read speed and subthreshold current of 2T memory cell. We perform our research on the basis of the whole memory cell, not only the anti-fuse device. The results can be directly used in PROM memory cell design application. We have also proposed a modified 3T memory cell. This structure consumes 18% more areas but it can improve the program consistency greatly.

2 Gate-oxide anti fuse PROM memory cell

2.1 Classic 3T memory cell

The most classic gate-oxide anti fuse memory cell is 3T cell. Most of the present mature gate-oxide anti-fuse PROM products are based on this structure. 3T cell consists of a N-type or P-type gate-oxide anti fuse, a high voltage block transistor and an address access transistor as showed in Fig. 1. High voltage transistor is used to

protect the address access transistor during the program mode. In the design, all cell transistors are N-type, in this way higher density has been got. With the standard CMOS 180nm technology, the area of 3T cell is $4.2 \mu m^2$. [4]

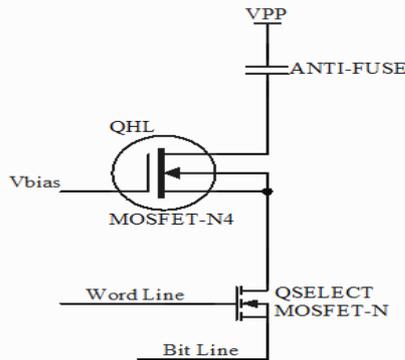


Figure 1. The structure of classic 3T cell

This structure has high reliability, the address access memory is well protected. But it has very cruel requirements on the size design of high voltage block transistor and address access transistor. What's worse, different technology requires different sizes. The design procedure consumes tremendous time and energy. The high voltage block is a device with thick oxide. This makes the cell consume many more areas. But very regrettably, the program consistency defect of gate-oxide anti-fuse cell has not been dealt with yet.

2.2 2T structure memory cell

Kilopass proposed the following 2T structure in Fig. 2. It consists of two identical N-type transistors. One is used as memory body, the other is the address access transistor. This structure reduces the design complexity substantially. At the same time, the cell's area and power consumption are also substantially reduced. In standard CMOS 180nm technology, the 2T cell we have designed consumes only $1.28 \mu m^2$.

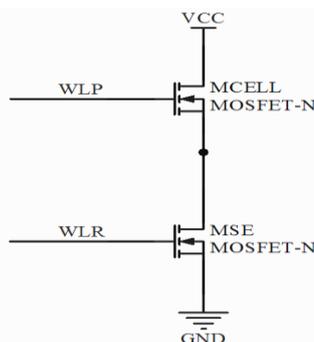


Figure 2. 2T memory cell

Compared to the classic 3T cell, the 2T cell has no high voltage block. During the program operation, high program voltage will break down the access transistor or have a negative effect on the access transistor's lifetime. So, we must avoid too high program voltage. The 2T cell also has the poor program consistency, which is the primary problem.

2.3 The choice of high density cell and research target

According to the results above, we have found that if the threat of high voltage can be resolved, the 2T cell is a very suitable choice for high density PROM. Therefore, we choose the 2T cell to do research on and consider the following two targets: (1) The failure situation of address access transistor. (2) The program consistency of the cell. We will obtain the best program of 2T cell after the study. On the basis of the 2T structure, we will trade off on the area consumption and modify the 2T cell structure to achieve better program consistency.

3 High density memory cell program performance study

3.1. Mechanism of gate-oxide anti fuse break down

When there are no defects in the S_iO_2 layer, the breakdown of the gate oxide is an avalanche breakdown. It corresponds to the impact ionization model. The original carriers accumulate enough energy due to the high electric field intensity. These carriers have impact on the lattice of S_iO_2 , generating secondary carriers-pairs of hole and electron. The secondary carriers generate next generation carriers. Carriers increase greatly and the current magnify in exponent. When the voltage come to the critical voltage, there is a sudden change in current. The gate oxide is irreversibly broken down. [4]

But there are no S_iO_2 layers which have no defects. So the intrinsic breakdown of gate oxide is an impact ionization-thermal transmission process. In the recent experiment, the test current has deviated from the normal F-N current and direct tunneling current under the added electric field intensity. With the increase of the added intensity, the test current increases obviously, it proves that the impact ionization has already occurred. But the heat generated is not enough for the medium fusing. Hence, after removing the added electric field, the medium can come back to the normal shape. With the increase of the added electric field intensity, the conduct currents mainly come from the filiform tubes formed by all kinds of defects. The heat generated can make the filiform tubes fusing and form the permanent conduct tunnel. The fusing state is testified by experiment. [5]

According to the impact ionization-thermal transmission model, the gate-oxide breakdown is a localized breakdown. Different breakdown spot positions correspond to different models.

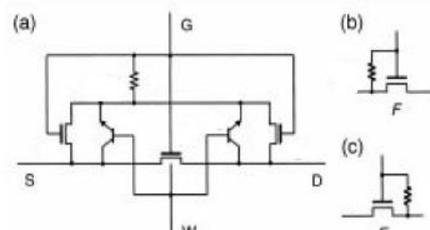


Figure 3. Three models of different breakdown spot position

From Fig. 3 [6], three mode are given:(a)the spot is in the channel(b)the spot is in the drain(c)the spot is in the source. From the cross-section of the programmed gate-oxide anti fuse, we can also find that the breakdown is a localized process.

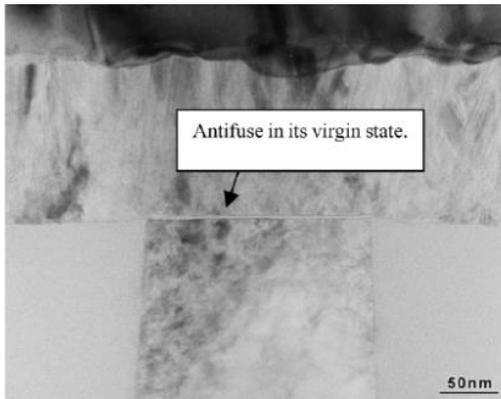


Figure 4. Cross-section of antifuse before program

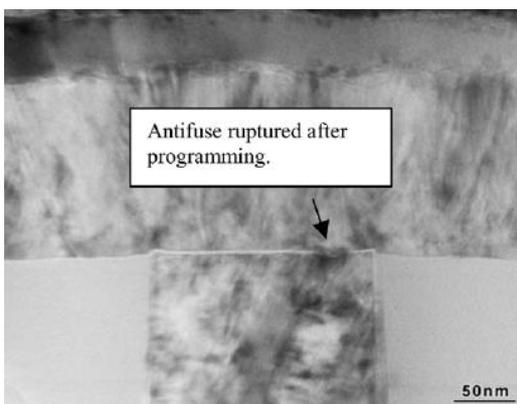


Figure 5. Cross-section of antifuse after program

The cross-sections in Fig. 4 and Fig. 5 certificate localized breakdown model and impact ionization-thermal transmission model [7]. The defects of the S_iO_2 layers are generated during the manufacture procedure. We can't orientate the defects' position right now. Therefore, we choose the program voltage as the main value and try the best to find the best program voltage. Further, we modify the 2T structure and consume more area. In this way, we have got a 3T cell structure, which improve the program consistency greatly.

3.2 The choice of program voltage

The program voltage is neither too high nor too low. The low voltage cannot break down the anti fuse or cost too much time. The high voltage may break down the address access transistor. So the program voltage has a feasible region: $[V_{min}, V_{max}]$.

Assume the programmed cell equivalent resistance is R , $R = \frac{V_{cc}}{I_{BL}}$, V_{cc} is the supply voltage, and I_{BL} is the current in the chosen Bit Line. Assume μ and σ the mean and standard deviation of the programmed cell equivalent resistance. The mean value is used to describe the power consumption and read speed. The standard deviation

value is to measure the program consistency. Obviously, the smaller σ is, the better consistency is. Considering the read speed and power consumption, The value of μ is acceptable in $[10k\Omega, 30k\Omega]$. [8] We give the model to be solved as follow:

Known that:

$$\sigma = f(V_{pp}), \mu = g(V_{pp}), V_{pp} \in [V_{min}, V_{max}]$$

To get $V_{pp,opt}$, which makes

$$\sigma_{min} = f(V_{pp,opt}), \mu = g(V_{pp,opt}) \in [10k\Omega, 30k\Omega]$$

The voltage effect on the cell program feature is derivate from the defects of gate oxide layers. The number and position of the defect, the heat needed for fusing contribute to the different electric features of the breakdown gate oxide. To a typical technology, the distribution of the defects has statistic laws. Thus, we can find the best program voltage for the corresponding technology. In this way, we can get the best program features of memory cell in the typical technology.

3.3 Modified 3T structure

Based on the 2T structure, we have proposed a 3T cell structure showed in Fig. 6. This structure adds a identical parallel NMOS as the memory body. This change makes the anti fuse break down more easily. The program consistency has improved a lot. It also improve the reliability of the address access transistor. The area of the 3T cell is $1.51 \mu m^2$ in standard CMOS 180nm technology. The 3T cell is still acceptable for high density design.

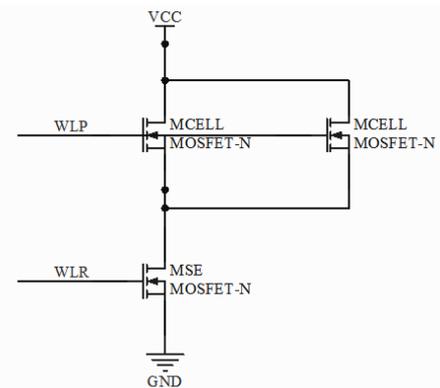


Figure 6. Modified 3T memory cell

4 Experiment design and results analysis

4.1 Preparation of test chips

The standard CMOS 180nm technology design rules are applied in the circuit design. To get better and more pure results of the cell program features, we have designed a 1×19 memory cell array showed in Fig. 7. It consists of nine 2T cells, 6 modified 3T cells and 4 other cells for further study. The schematic is below. The chip is packaged in DIP28.

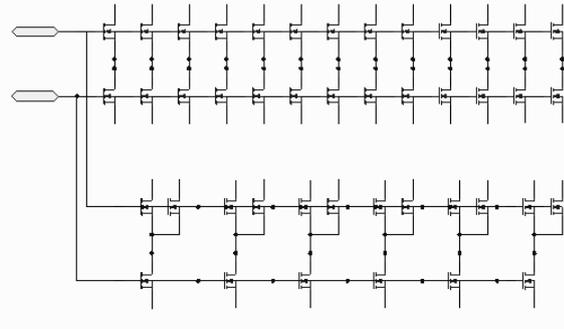


Figure 7. Schematic of test chip

4.2 Experiment scheme

(1) The set of the voltage value

The intrinsic gate oxide breakdown voltage is 5.8V [4] in 180nm standard CMOS technology. Considering the voltage drop in the test chip and the deviation, we choose 6V, 6.5V, 7V, 7.5V, 8V for study.

(2)Experiment procedure

- 1) 25 test chips in total. Read the cell memory before program, record the bit line current.
- 2) 5 test chips per voltage, do program operation on each chip and read the cell after program. Record the bit line current after program.
- 3) Analyze the test data and get the result.

4.3 Experiment results

4.3.1 8V circumstance

The 8V program voltage made the address access transistor break down in each chip. Thus, $8V > V_{max}$. Due to the $\pm 0.25V$ deviation, we assumed that $7.75V \geq V_{max}$. It shows that if the program voltage is too high, the address access transistor may be broken down and the circuits fail.

4.3.2 6V circumstance

Under the 6V program voltage, only 3 memory cell broke down in the total 5 chips. It was the early breakdown phenomenon which can be eliminated through screening. The result tells that $6V < V_{min}$. Because of the $\pm 0.25V$ deviation, we assume that $6.25V \leq V_{min}$.

4.3.3 6.5V,7V,7.5V circumstances

The three voltages all give the correct program results. Therefore, we got:

$$V_{min} < 6.5V < 7.5V < V_{max} \quad (1)$$

Due to $\pm 0.25V$ deviation, we assume that:

$$V_{min} \leq 6.25V < 7.75V \leq V_{max} \quad (2)$$

According to the results of 6V and 8V results, we can get the feasible region of program voltage: $[6.25, 7.75]V$.

After dealing with the data, the results are as follows: the distributions of equivalent resistances are showed in Fig. 8, 9 and 10.

(1)6.5V circumstance

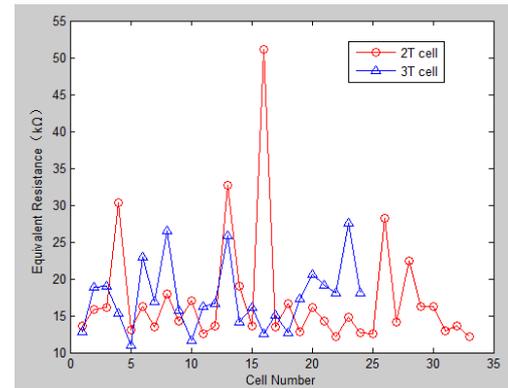


Figure 8. 6.5V voltage 2T structure and 3T structure equivalent resistances distribution

2T structure: $\sigma = 7.9079k\Omega, \mu = 17.3479k\Omega$

3T structure: $\sigma = 4.5402k\Omega, \mu = 17.5330k\Omega$

(2)7V circumstance

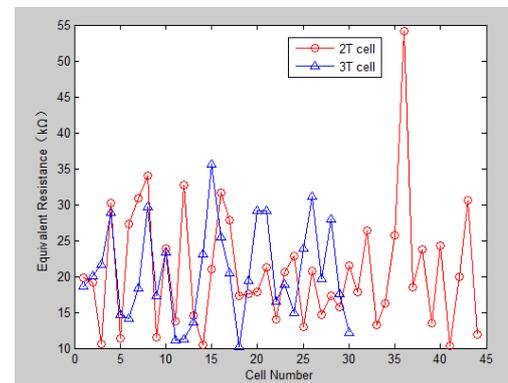


Figure 9. 7V voltage 2T structure and 3T structure equivalent resistances distribution

2T structure: $\sigma = 8.4118k\Omega, \mu = 20.7058k\Omega$

3T structure: $\sigma = 6.7020k\Omega, \mu = 20.6003k\Omega$

(3)7.5V circumstance

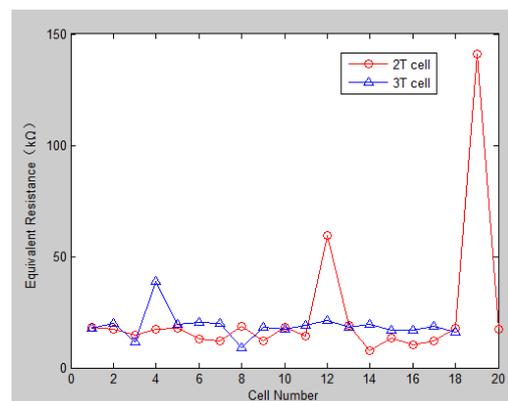


Figure 10. 7.5V voltage 2T structure and 3T structure equivalent resistances distribution

2T structure: $\sigma = 29.5480k\Omega, \mu = 23.5483k\Omega$

3T structure: $\sigma = 5.8086k\Omega, \mu = 18.8656k\Omega$

4.4 Results analysis

First of all, the feasible region of program voltage is $[6.25, 7.75]V$.

Due to the $\pm 0.25V$ deviation, we can ensure $V_{pp,opt}$ from 6.5V, 7V and 7.5V. Under the three program voltages, the mean values of 2T cell equivalent resistances are all in $[10k\Omega, 30k\Omega]$, fulfilling the requirements. The parameter σ which measures the program consistency is $7.9079 k\Omega$, $8.4118 k\Omega$, $29.5480 k\Omega$ under 6.5V, 7V and 7.5V. It accords with the exponent model approximately: With the increase of program voltage, the cell program consistency performance decrease in exponent. The mean values of modified 3T cells are also in $[10k\Omega, 30k\Omega]$. The largest value of 3T structure's σ is $6.7020 k\Omega$. The value is 15.3% less than the 2T's best situation. The 3T cell consumes 18% more area. 15.3% is the worst case. The consistency can be improved 80.3% in 7.5V circumstance. Finally, we ensure $V_{pp,opt} = 6.5V$.

5 Conclusion

The program features of the 2T high density PROM gate-oxide anti-fuse memory cell have been studied in this paper. We have built a model for the programmed memory cell equivalent resistances. With the model, we have assessed the memory cell program consistency. The effect of the program voltage has also been researched. The result showed that lower program voltage made better cell program consistency in 2T cell. The best program voltage was 6.5V for 2T cell. After trading off between power consumption and read speed, the programmed cell equivalent resistance was between $[10k\Omega, 30k\Omega]$. A modified 3T structure was proposed to improve the cell program consistency. The proposed cell

consumed 18% more area. The standard deviation of the 3T cell equivalent resistances after program decreased 15.3% in the worst case. It could decrease 80.3% at most. The cell program consistency was improved greatly.

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