Research on and design of key circuits in RFID tag chip for container management

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Abstract: This paper introduces the design of semi-passive RFID tag chip capable of monitoring container safety. A system framework complying with requirements by ISO/IEC 18000-6C is firstly presented, and then differences from the key units of common passive chip, such as switch-state monitoring circuit, power management unit and anti-shake design in baseband processor, are elaborated. The main function of such a chip is to record the container opening frequency during transportation. Finally, the realizations of each unit's function are simulated.

1. Introduction

With the development of RFID technology, mere identification of target objects can not satisfy the various application needs; thus, embedding a sensor unit into the RFID tag chip to monitor the environment of objects has great significance in the application fields, such as logistics and supply chain management. In recent years, several RFID tag chips inserted with temperature sensors have been proposed [1]-[4]. To meet the specific requirement in the application fields, tag chips with various special features have become a research focus and developing trend of the RFID technology. However, no such RFID tags that can monitor the transportation safety and the logistics industry where RFID is widely used urgently needs have been developed.

2. System Framework

Fig. 1 is the block-diagram of the chip system [5], [6], including Power Management Unit (PMU), Switch-state Monitoring Unit (SSM), ASK demodulator, modulator, POR, oscillator, baseband processor and memory. The PMU consists of recertification circuit, voltage regulator circuit, and wake-up circuit. The rectification circuit converts the received RF energy into DC voltage which will then be stabled by the voltage regulator circuit at 1V and 1.8V to support for the operation of other units; while the wake-up circuit controls the power supply based on the strength of chip's received RF energy, which increases the effective working distance and concomitantly minimizes the battery consumption. SSM monitors the state of the container switch through initiating battery activation tag and sending a signal "Son" when the switch state changes. Then the baseband processor starts to count when receiving the signal "S_{on}", and stores the counted values in the memory; after that, the processor will send signal "P_{ctl}" to switch off the battery, following which the chip will turn to sleep. Functions and designs of the recertification circuit, voltage regulator circuit, ASK demodulator, modulator, oscillator and POR are the same as those of passive chip. What different from the common passive chip are the designs of PMU, baseband processor and SSM, which will be elaborated in the following.

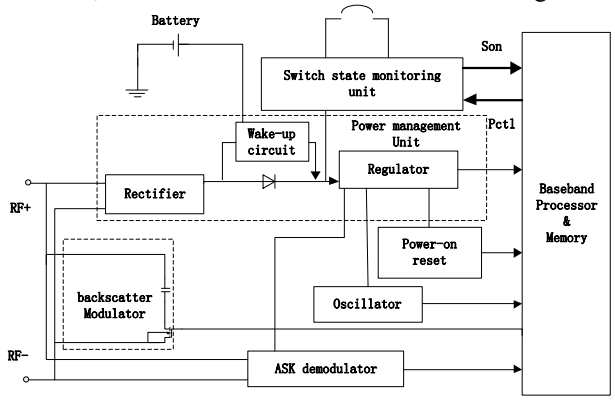

Figure 1. Block diagram of a special label system for container management

3. Ultra-low-consumption Switch-state Monitoring Circuit

Fig. 2 (a) is a schematic diagram of the switch-state monitoring circuit with cores of switching tube T1 and control logic. Switch S, representing the state of the container switch, jointly controls the state of the battery with T1. When S and T1 are simultaneously turned on, the battery will provide power to chip to make it work. Inverters Inv2 and Inv3 can transform the levels of signals, changing the signal S_{on} level to 1V. Other control

logic units are directly powered by the battery. Therefore, the high level of signals "P_{ctl}" and "S_{on}" is 1V, and 3V for others (CR2032 battery voltage).

Fig. 2 (b) shows the sequence diagram of the switch-state monitoring circuit. When the switch S disconnects, the chip cannot get battery power with P_{ctl} of low level, V_{en} of high level, V_g and V_a of same low level, so T1 is in conducting state. When the switch S closes, V_{en} is low and the latch D stops working and T1 remains conductive, then the battery can supply power to the chip to make it work through the switches S and T1, and the level of S_{on} becomes higher, baseband processor starts counting and send P_{ctl} to turn off T1 to switch off the battery, and the tag turns to sleep [7]. Thus, whenever the switch state is changed, the chip only works several milliseconds for counting in the whole process, i.e. V_b is at a high level in Figure. 2 (b), and only control circuit of SSM keeps working during the remaining time, which greatly extends the service life of the battery.

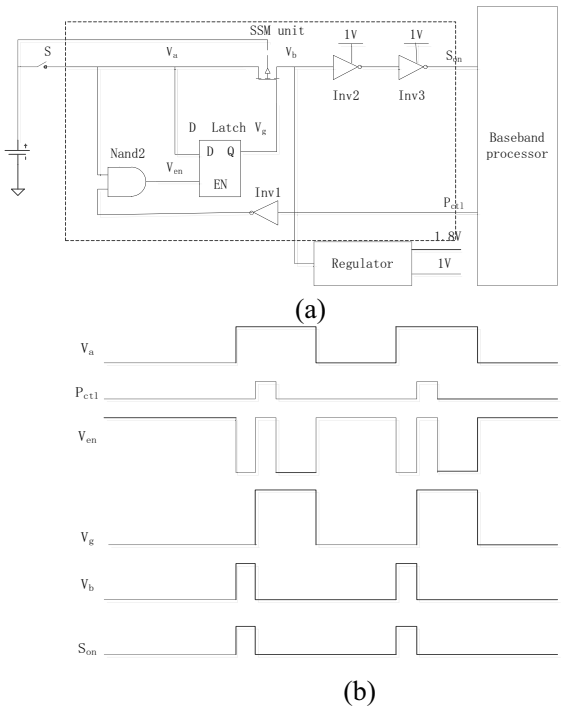

Figure 2.Switch status monitoring circuit

(a) switch status monitoring circuit schematic; (b) main signal timing diagram

4. Power Management Unit

The PMU consists of rectification circuit, voltage regulator circuit, and wake-up circuit; among which the former two have the same functions as those of the passive chip. The wake-up circuit is a specific module for passive chip that can change the power supply mode based on the strength of received RF energy; which can increase the working distance of chip on the one hand and decrease the consumption to extend the service life [8], [9] of battery on the other hand.

The wake-up circuit consists of two independent sub-circuits that control the two output terminals of rectification circuit respectively. Fig. 3 shows the schematic diagram of one circuit in which V_{REC} connects with the output terminal of rectification circuit, V_{bat} with the positive electrode of battery, and V_O with the input terminal of voltage regulator circuit. The serial resistance divider (which can be diode-connected MOS instead) connecting with V_{REC} divides the output voltage of rectification circuit proportionately that generates two voltage signals i.e. V_{sel1} and V_{sel2}. V_{sel1} equaling to $0.75V_{REC}$ connects with inverter INV1, while V_{sel2} equaling to 0.25 V_{REC} connects with inverter INV2. Threshold voltages of the two inverters are represented by V_{m1} and V_{m2} respectively. Only when $V_{sel1} > V_{m1}$ and $V_{sel2} < V_{m2}$ (namely $4\ V_{m1}/\ 3 < V_{REC} < 4V_{m2}$), the grid potential of PMOS MP is low, and MP is turned on, then the battery can feed the voltage regulator circuit that will then supply power to chip with 1V and 1.8 V. In other cases, the battery will be turned off, namely only the output voltage V_{REC} is within the specified range said above can the battery supply power. The minor value (V_{min}) is determined by the sensitivity of ASK demodulator. For this design, the minimum RF signal amplitude that the demodulator can correctly demodulate is 300mV; to leave a certain margin, the output voltage of the rectification circuit when the input RF signal amplitude is 160mV is set as V_{min}; the major value (V_{max}) is able to meet the minimum required output voltage for normal operation [10]. With this design, the battery will be turned on only when the RF energy received reaches the sensitivity of ASK demodulator but not enough to activate the chip; which can increase the working distance of the chip with no waste of battery energy. In this design, the battery will be turned on when $0.3V < V_{RECL} < 1.1V$ or $0.4V < V_{RECH} < 2V$.

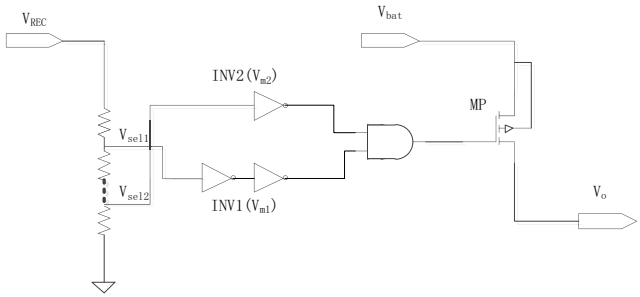

Figure 3.Power management module block diagram

5. Baseband Processor

The special tag baseband processor herein shown in Fig. 4, consists of decoder, encoder, CRC module, timing synchronization module, memory read-write control module, random-number generator, collision arbitration module and finite state machine, etc.; among which, the finite state machine is the core that consists of de-jitter circuit, switching frequency recording module, state-machine-enabled module, synchronization circuit, command processing module and Mealy-type finite state machine. In addition to performing a series of commands and operations specified by protocol, the processor is also required to record the switching frequency. As there is dither signal that may cause error count when a

mechanical switch is switching, this paper designs a de-jitter circuit to eliminate the effects.

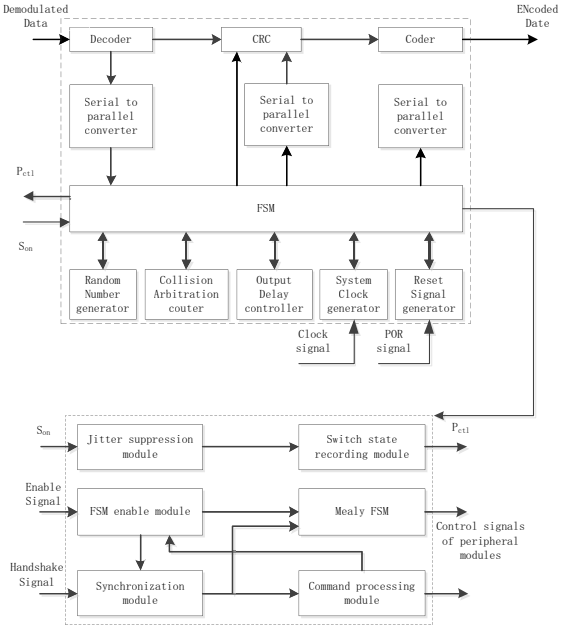

Figure 4.Block diagram of baseband processor system

The fundamental principle for the de-jitter circuit is to use a bidirectional counter, as shown in Figure 5, that can sample signals "S_{on}", and conduct addition or subtraction to the counter values respectively based on the high level or low level of "S_{on}" [11]-[13]. If the signal "S_{on}" is under high level, the counter will count the clock pulses and pull the "S_{ons}" high when the count value reaches the set standard. Conversely, if the signal "S_{on}" is under low level, the counter will do the subtraction to the count value till zero and pull the "S_{on}" low. As shown in Fig. 5, this method effectively eliminates the effects by dither signals and improves the system reliability.

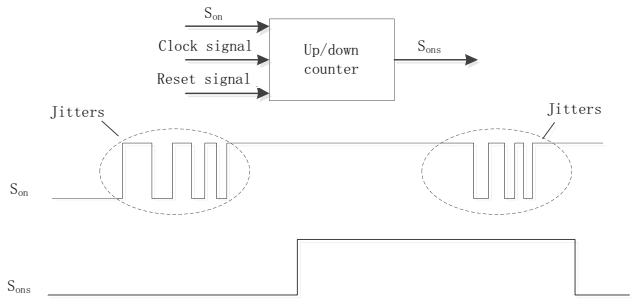

Figure 5. Schematic diagram of the working principle of the jitter circuit

6. Simulation Analysis

The chip adopts TSMC 0.18μm CMOS design, and Figure 6 shows the complete chip layout. The analog circuit uses Spectre for simulation analysis, and the chip consumes 9.56μW while working.

Simulation results of SSM are shown in Fig. 7. The delay time of the unit is 92μs and will not have negative effects on the system due to the low switching frequency. Part of the control logic of SSM and PMU is directly fed by the battery, so there is still very low power consumption while the tag is in sleep mode, and the quiescent current under this mode is only 645 pA according to the simulation results

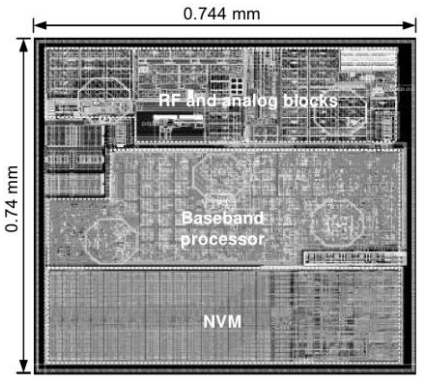

Figure 6 .Special label chip layout

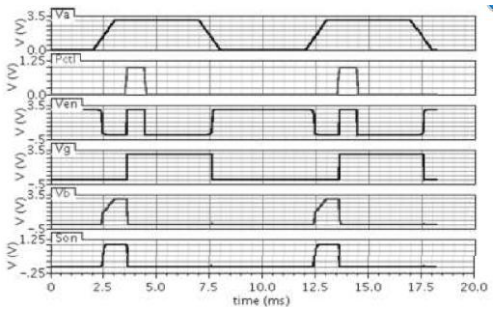

Figure 7.The simulation waveform of the key signal in the switch state monitoring circuit.

Fig. 8 shows the co-simulation waveform of PMU, rectification circuit and voltage regulator circuit, wherein V_{RECL} is the low output voltage of the rectification circuit, Reg_out_low is the low output voltage of the voltage regulator circuit (1V), and Reg_in_low is the low input voltage of the regulator circuit. It is obvious that Reg_in_low is zero when the rectification output voltage is very low initially, and the battery is turned off; then, as the rectification output voltage rises, when 0.3V <V_{RECL} <1.2V, namely the tag is in the RF field but receives insufficient RF energy, the battery will be turned on to feed the Reg_in_low (Reg_in_low is the battery voltage of about 3V); Finally, when the rectification output voltage rises and stabilizes at about 1.4V, as V_{RECL}> 1.2V and the battery turns off, the voltage regulator circuit will still be activated by the rectification circuit (Reg_in_low = V_{RECL}).

As the diode-connected MOS plays as the serial resistance divider of wake-up circuit as well as inverter, the deviation between the divided voltage proportion and the inverter threshold is small due to the same effects on MOSs from TT, FF and SS process corners and different temperatures. However, since the fluctuations of supply voltage will affect the values of the divided voltages V_{sel1} and V_{sel2} of rectification output voltage, and the threshold voltage of inverter, the circuit will be affected by changes of the operating voltage (battery voltage) to some extent

[14-16].It shows the simulation results of the turning on/off threshold voltages of the wake-up circuit under different battery voltages. Wherein, bat_low_on and bat_low_off are the turning on threshold voltage and turning off threshold voltage of the wake-up circuit of regulated low input terminal respectively; while bat_high_on and bat_high_off are the turning on threshold voltage and turning off threshold voltage of the wake-up circuit of the regulated high input terminal respectively. Visibly, as the battery voltage increases, the threshold voltage of the wake-up circuit will increase to some extent, but the fluctuations of the turning on/off thresholds will not affect the normal operation of the chip [17].

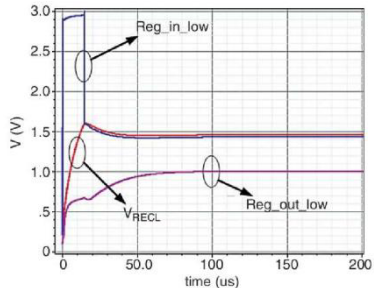

Figure 8. Power management module simulation waveform

7. Conclusion

With the wide application of RFID technology, people put forward higher demands for the functions of RFID chips, such as monitoring the environment of objects through embedding the sensors in the chip, which is significant to logistics and supply chain management and other fields. This paper introduces a design of special tag chip for container management. It can record the opening frequency of container during transportation and comply with requirements by ISO/IEC18000-6C. The major difference between this chip and the common passive tag chip lies in the system framework, switch-state monitoring unit, power management unit and anti-shake design in baseband processor. Thus, this study focuses on those abovementioned aspects, and the corresponding simulation results are discussed.

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