

# Hardware Design of Tuber Electrical Resistance Tomography System Based on the Soil Impedance Test and Analysis

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**Abstract.** The hardware design of tuber electrical resistance tomography (TERT) system is one of the key research problems of TERT data acquisition system. The TERT system can be applied to the tuber growth process monitoring in agriculture, i.e., the TERT data acquisition system can realize the real imaging of tuber plants in soil. In TERT system, the imaging tuber and soil multiphase medium is quite complexity. So, the impedance test and analysis of soil multiphase medium is very important to the design of sensitive array sensor subsystem and signals processing circuits. In the paper, the soil impedance test experimental is described and the results are analysed. The data acquisition hardware system is designed based on the result of soil medium impedance test and analysis. In the hardware design, the switch control chip ADG508, the instrumentation amplifier AD620 and programmable amplifier AD526 are employed. In the meantime, the phase locked loop technique for signal demodulation is introduced. The initial data collection is given and discussed under the conditions of existing plant tuber and no existing plant tuber. Conclusions of the hardware design of TERT system are presented.

## 1 Introduction

Tuber electrical resistance tomography (TERT) originates from industrial ERT technology. TERT system is aimed to extend the application of the technology into agriculture, which could be used in monitoring the status of tuber growth, breeding new varieties of plant tubers and fine cultivation. Compared with the traditional ERT system, TERT system pays more attention to the image reconstruction quality rather than the data acquisition rate. Thus the hardware design of TERT data acquisition, especially in excitation and measurement strategies, is also different from the industrial ERT system [1].

The structure of TERT system showed as Fig. 1 contains: excitation current source module, sensitive array sensor subsystem, switching control module, signal conditioning module and computer of image reconstruction [2]. The data acquisition mode of the system is adjacent mode with four electrodes [3], which is a widely application data acquisition mode in ERT system. There are sixteen electrodes in one layer, and it will get boundary voltage values in adjacent mode [4].

The sensitive array sensor subsystem is 16 electrodes system in adjacent mode, which designed by our research group [5]. The container's diameter is 300mm, and with an electrode array of 6×16 electrodes on the inner wall. The material of the electrodes is titanium, which provides a good electrical conductive performance and corrosion proof. As the overall electrodes are manufactured by using wire-electrode cutting technique, there is no effect of welding stress and deformation. In addition, the

electrodes are made by using chamfering dovetail sink whole process, and adhesive on the container with special glue, this made the device has a good water proof and immersion proof performance. The customized connect cable has very small impedance value and excellent anti-jamming performance.

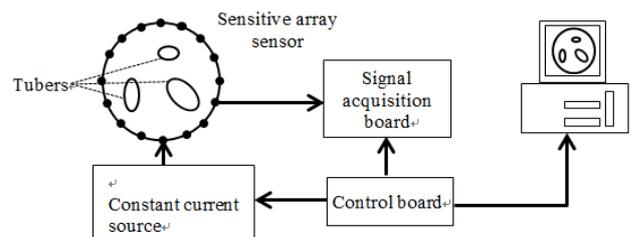


Figure 1. TERT system structure.

## 2 Soil impedance test and analysis

The measured objective field-the medium of soil in the TERT system is different from which of traditional ERT system. Its resistivity numerical is high, distribution is not homogeneous, and humidity impact, soil quality and other factors cannot be ignored [6]. So, in the hardware design of TERT data acquisition system, the soil impedance characteristics test and analysis is needed.

The test of soil impedances in different moisture content is completed. It gives a basic range of soil impedance and provides a reference in the hardware design. Then the voltage values between the electrodes

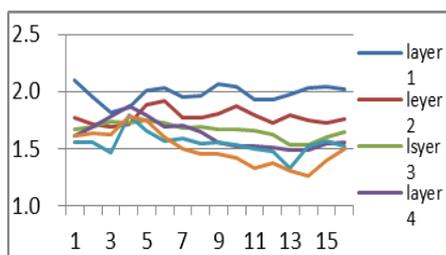
are measured, this will provide a basic acknowledge of amplification ratio for the subsequent circuits design. The experimental instruments are HP-4284A impedance tester and the 34401A digital multimeter with 61/2 digital resolution. The picture of the test is shown in Fig. 2.



**Figure 2.** Soil impedance test.

### 2.1 Soil impedance test

In the Quasi-static field theory, it requires the medium of the field is homogeneous [7]. However, the absolutely homogeneous soil is difficult to achieve because soil multiphase medium is rather complexity. Before the soil impedance formal test the first thing is finding out the ratio of soil and water in saturated soil. The detailed measuring process is: the impedance of adjacent electrodes is continuously measured while water is adding into the container with sensitive array electrodes progressively; when the impedance value of adjacent electrodes is no longer change, which means the soil has reached the saturated state, and then the ratio of water is just about 10.71%. The next is the formal soil impedance test. The measured data in saturated soil is showed in Table 1. It can be drawn in curve graphs as shown in Fig. 3.



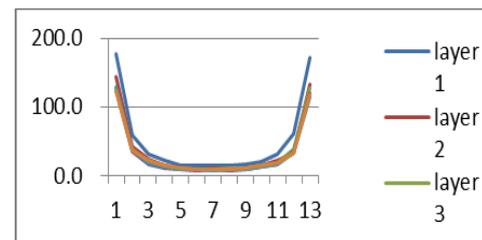
**Figure 3.** Impedance tested in saturated soil.

From Fig. 3, it can be seen that the resistance of saturated soil is between 2.1kΩ and 1.3kΩ. And the soil impedance (resistance value) decreases according to the decreasing of layers' number. The distribution of soil impedance (resistance) is relatively uniform, which is much better than the dry soil, it reaches the requirement of quasi-stationary field theory.

### 2.2 Measurement of the boundary voltage between each two electrodes

The experimental test aims to get the range of boundary voltage output, and it can provide important guidance in the hardware design. The excitation current source for the test is 30mA, 5 KHz sine wave. The measured voltages

between electrodes are shown in Table 2, and the drawn curves are shown in Figure 4.

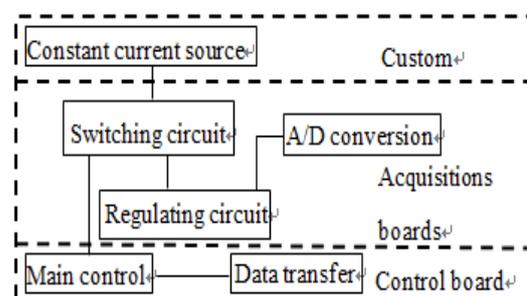


**Figure 4.** Adjacent electrode voltage change curves.

From the Figure 4, it can be seen that the tendency of voltage values change, i.e., it reduces first and then enlarge symmetrically, it meets the requirement of quasi-stationary field theory, and is in the range of more than a dozen mV and a few hundred mV. As is shown that the maximum voltage value is ten or fifteen times than the minimum one, programmable amplifier circuit should be designed in the data acquisition system.

## 3 Data Acquisition System Design

The hardware of TERT system is mainly including three parts: constant current source, one signal acquisition board for each layer, and one board of main control circuit. The constant current source can produce sine excitation current signal, and it is designed based on the impedance characteristic of the array electrodes sensing subsystem. There are six pieces of signal acquisition board; each board is used to collection the boundary voltage of one layer's electrodes. As the central control part, the main control circuit board is responsible for the switching process and data transfer control of the whole system [8]. Power supply is also provided on the main control circuit board. Overall system composition is shown in Fig. 5.



**Figure 5.** Signal acquisition board architecture .

### 3.1 Hardware design

#### 3.1.1 Switching circuit

Because the soil impedance is greater than the traditional medium impedance of ERT system, three things should be taken into consideration. First, the intensity of excitation current single should be increased; second, in order to control the bigger excitation current single, the

switching chip should withstand a higher voltage value; last, TERT system in data acquisition is more concerned with accuracy, reliability, and less noise ratio rather than speed. So the switching circuit is different from the traditional ERT system. In the switching process design, relays and switching chip ADG508, which is CMOS monolithic analog multiplexers with 8 channels, are employed. The switching circuit for one channel is shown in the Fig. 6.

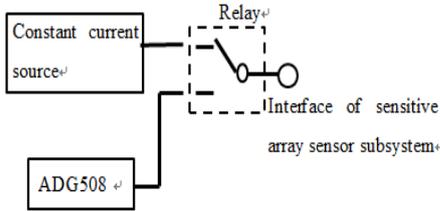


Figure 6. Switching circuit for one channel.

### 3.1.2 Amplifier and Filter

This part includes three parts: differential operational amplifier circuit, low pass filter circuit, and programmable amplifier circuit. Differential amplifier circuit is used to preliminary amplifier the voltage between electrodes and to make the two way signal input into one way signal output. The AD620, a three-transport discharge scale amplifier chip, is used as a 20 times the first level of amplification [9]. After the differential operational amplifier circuit, a fourth-order filter, which is consisted by two second-order Butterworth filter is used to removing the high-frequency noise introduced by the electronic switch, which always up to a few MHz. Then the AD526, single-chip software programmable gain amplifier, is used to amplify the signal. The AD526 can realize a gain of up to 16 multiples, which covered the multiple among the voltage values, obtained in one ring collection, and it can amplify the voltage values into a similar voltage range effectively.

### 3.1.3 Multiplication demodulation

In order to convert the AC signal into a DC signal the multiplication demodulation method is used in the system. The Schematic diagram of multiplication demodulation is shown in Figure 7.

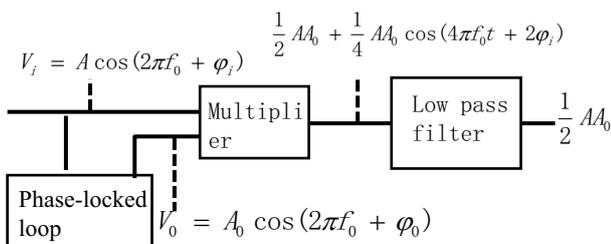


Figure 7. Schematic diagram of multiplication demodulation .

Suppose the demodulated signal is  $V_i = A \cos(2\pi f_0 t + \phi_i)$ , the reference signal is

$V_0 = A_0 \cos(2\pi f_0 t + \phi_0)$ , and  $V_i$  multiply  $V_0$  can get  $V$  :

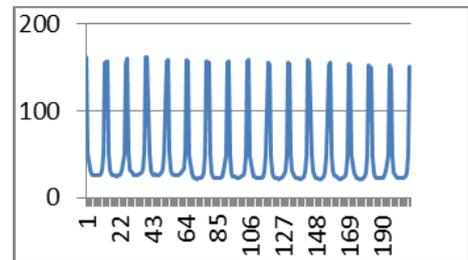
$$V = \frac{1}{2} AA_0 \cos(\phi_i - \phi_0) + \frac{1}{4} AA_0 \cos(4\pi f_0 t + \phi_i + \phi_0) \quad (1)$$

where  $\phi_i$  is the phase of the demodulated signal;  $\phi_0$  is the phase of the reference signal;  $f_0$  is the frequency of both demodulated signal and reference signal.

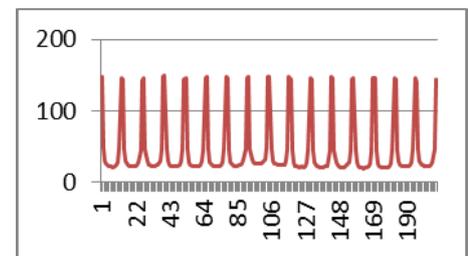
MAX297 chip with an 8th-order switched-capacitor filter function is used to filter out the AC signal expressed in formula (1). In order to get a higher precision, a phase-locked loop is used in the system to insure  $V_0$  has a same phase with  $V_i$ , this will make  $\cos(\phi_i - \phi_0) = 1$  in formula (1) [10], and get the largest dc component.

### 3.2 Initial data collection test and results analysis

In order to determine the feasibility and rationality of the designed hardware of TERT system, the boundary voltages between each two electrodes are measured. The data collection test (only the third layer electrodes) is completed in the condition of existing plant tuber or not in the TERT system. The initial test results are shown in Fig. 8.



a. No exist plant tuber.



b. Exist plant tuber.

Figure 8. Boundary voltages test of TERT system in existing plant tuber or not.

From Figure 8, it can be seen that the boundary voltages data and curves are very similar to the traditional ERT system. So, after the accurate circuit amplifying, filtering, and signal multiplication demodulating, the image reconstruction of plant tuber by using specific imaging algorithm can be realized.

## 4 Conclusion

In the soil impedance experimental test and the hardware design, it can be drawn the following conclusions: the ratio of water is about 10.71% in the saturated soil of the test; the impedance value of saturated soil is between 2.1k $\Omega$  and 1.3k $\Omega$ ; the boundary voltage between each adjacent two electrodes is in the range of more than a dozen mV and a few hundred mV, and the maximum voltage value is ten or fifteen times than the minimum one. Based on the saturated soil impedance test, in the hardware design, the customized excitation current source with 30mA, 5 KHz sine wave and the switching circuit with both relays and switching chips are selected; based on the test of boundary voltage characteristics of the TERT system, the amplifier with a 20 times' three-transport discharge scale amplifier and a software programmable gain amplifier are employed; then a multiplication demodulation based on the phase-locked loop is adopted to transform AC signal into a DC signal. The soil impedance test provides the basis of hardware design, and the initial data collection test verifies the rationality of hardware design.

## Acknowledgement

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