The Design of Phase-Locked-Loop Circuit for Precision Capacitance Micrometer

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Abstract. High precision non-contact micrometer is normally divided into three categories: inductance micrometer, capacitance micrometer and optical interferometer micrometer. The capacitance micrometer is widely used because it has high performance to price ratio. With the improvement of automation level, precision of capacitance micrometer is required higher and higher. Generally, capacitance micrometer consists of the capacitance sensor, capacitance/voltage conversion circuit, and modulation and demodulation circuits. However, due to the existing of resistors, capacitors and other components in the circuit, the phase shift of the carrier signal and the modulated signal might occur. In this case, the specific value of phase shift cannot be determined. Therefore, error caused by the phase shift cannot be eliminated. This will reduce the accuracy of micrometer. In this design, in order to eliminate the impact of the phase shift, the phase-locked-loop (PLL) circuit is employed. Through the experiment, the function of tracking the input signal phase and frequency is achieved by the phase-locked-loop circuit. This signal processing method can also be applied to tuber electrical resistance tomography system and other precision measurement circuit.

1 Introduction

When measuring the micro displacement with the capacitive sensor, in addition to the weak measurement signal, there are also other noise signals. In order to distinguish measurement signal from noise signals, method of modulating the useful signal is used. In this design, amplitude modulation is employed. At receiving end, modulated signal is demodulated, and the measured signal is eventually reduced. Phase sensitive detection circuit is used in this design. The system block diagram of this design is shown in Fig. 1.

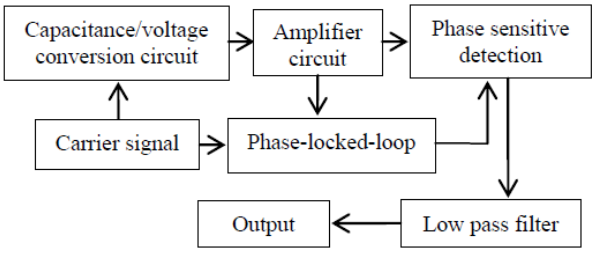

Figure 1. The system block diagram of measurement circuit.

The measured signal is loaded onto the carrier signal, after the capacitance/voltage conversion circuit, the corresponding voltage signal is obtained. In the process of signal transmission, phase shift will be occurred, due to the existing of resistors, capacitors and etc. In order to improve the accuracy of phase sensitive detection, PLL circuit is added. The function of the PLL is making the two signals of the input of phase sensitive detection with the same frequency and same phase. Thereby the output precision of phase sensitive detection and the accuracy of the measurement results will be improved.

2 The principle of PLL for demodulation circuit

Amplitude modulation is widely used because of simple circuit. Carrier signal is generated by the Wien bridge oscillator in this design. The general expression of the linear amplitude modulation signal is:

$$u_s = (U_m + mx)\cos\omega_c t \tag{1}$$

where: ω_c is the angular frequency of the carrier signal, U_m is the amplitude of the carrier signal, and m is modulation depth [1].

In order to obtain the measured signal, the demodulation circuit is needed. There are two ways to demodulation: the envelope detector and phase sensitive detector. In order to make the circuit have the ability to determine the phase and frequency of signal, improve the ability of anti-interference, phase sensitive detection circuit is used. In general, the block diagram of phase sensitive detection system consists of multiplier circuit shown in Fig. 2.

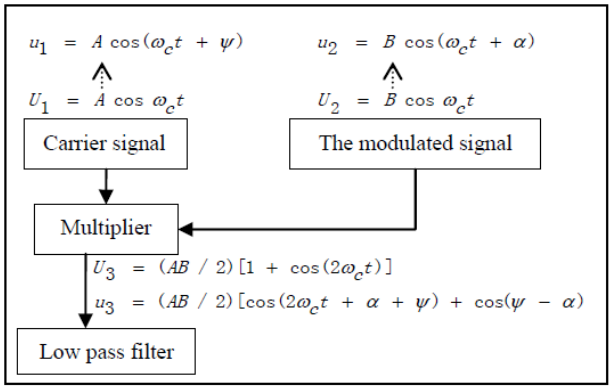

Figure 2. The block diagram of phase sensitive detection system.

Two inputs of the multiplier are carrier signal and the modulated signal. Under the ideal conditions, the carrier signal is written as:

$$U_1 = A\cos\omega_c t \tag{2}$$

where: A is amplitude of carrier signal.

The modulated signal is expressed as:

$$\begin{aligned} U_2 &= (U_m + mx)\cos\omega_c t \\ &= B\cos\omega_c t \end{aligned} \tag{3}$$

where: B is amplitude of the modulated signal.

The output of multiplier is:

$$\begin{aligned} U_3 &= AB\cos\omega_c t\cos\omega_c t \\ &= \frac{AB}{2}[1 + \cos(2\omega_c t)] \end{aligned} \tag{4}$$

In practice, the phase shift will occur in circuit. The phase shift of the carrier signal is ψ, the phase shift of the modulated signal is α, then:

$$u_1 = A\cos(\omega_c t + \psi) \tag{5}$$

$$\begin{aligned} u_2 &= (U_m + mx)\cos(\omega_c t + \alpha) \\ &= B\cos(\omega_c t + \alpha) \end{aligned} \tag{6}$$

Under such circumstances, the output of the multiplier is drawn as:

$$\begin{aligned} u_3 &= AB\cos(\omega_c t + \psi)\cos(\omega_c t + \alpha) \\ &= \frac{AB}{2}[\cos(2\omega_c t + \psi + \alpha) + \cos(\psi - \alpha)] \end{aligned} \tag{7}$$

According to formula (7), even if the high frequency signal is filtered by the low pass filter, the output is also related to the size of the phase shift. In order to eliminate the impact caused by the phase shift, the phase-locked-loop is added in this design.

The system block diagram of phase-locked-loop method is shown in Fig. 3 [3].The principle of PLL is using the phase difference between two signals to control the frequency of the output signal of the voltage controlled oscillator (VCO). Ultimately, the frequency of the output signal equals to the input signal, and the phase difference is zero or a fixed value. The input signal is described as:

$$u_i(t) = U_{im}\sin[\omega_i t + \varphi_i(t)] \tag{8}$$

where: ω_i is instantaneous oscillation angular frequency, and $\varphi_i(t)$ is instantaneous phase.

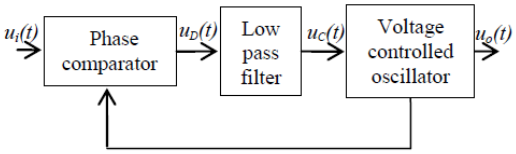

Figure 3. The system block diagram of phase-locked-loop method.

The output of the VCO can be obtained:

$$u_o(t) = U_{om}\cos[\omega_o t + \varphi_o(t)] \tag{9}$$

where: ω_o represents natural oscillation angular frequency, and $\varphi_o(t)$ is instantaneous phase.

The output of the phase comparator is [5]:

$$u_D(t) = Ku_i(t)u_o(t) \tag{10}$$

The output of the low pass filter is described as:

$$u_C(t) = \frac{1}{2}KU_{im}U_{OM}\sin[\omega_I t + \varphi_I(t) - \omega_O t - \varphi_O(t)] \tag{11}$$

The relationship between the instantaneous frequency and phase is written as:

$$\omega(t) = \frac{d\theta(t)}{dt} \tag{12}$$

From formula (12), it can be deduced:

$$\theta(t) = \int \omega(t)dt + \theta_{d0} \tag{13}$$

Instantaneous phase difference is:

$$\theta_d = (\omega_i - \omega_0)t + \varphi_i(t) - \varphi_o(t) \tag{14}$$

After differential, we can get:

$$\frac{d\theta_d}{dt} = \frac{d(\omega_i - \omega_0)t}{dt} + \frac{d[\varphi_i(t) - \varphi_o(t)]}{dt} \tag{15}$$

When formula (15) is zero, the frequency of output equals to the input, and the phase difference is zero or a fixed value.

In this design, the phase-locked-loop method is applied to the demodulation circuit, and the system block diagram is shown in Fig. 4. From the above analysis, we know that u_4 and u_2 are signals with the same frequency and same phase. So the output of multiplier is written as:

$$\begin{aligned} u_5 &= BC\cos(\omega_c t + \alpha)\cos(\omega_c t + \alpha) \\ &= \frac{BC}{2}[\cos(2\omega_c t + 2\alpha) + 1] \end{aligned} \tag{16}$$

Then the output of low pass filter is:

$$u_6 = \frac{BC}{2} \tag{17}$$

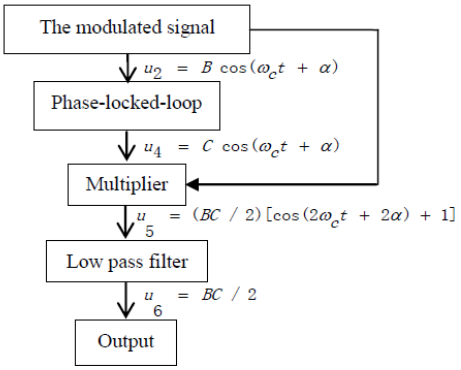

Figure 4. The system block diagram of improved demodulation circuit.

3 The parameters design of PLL circuit

CD4046 chip is employed in the PLL circuit design. The low pass filter of PLL circuit requires external connecting of resistors and capacitors [6]. The left picture of Fig. 5 shows the diagram of the designed PLL circuit.

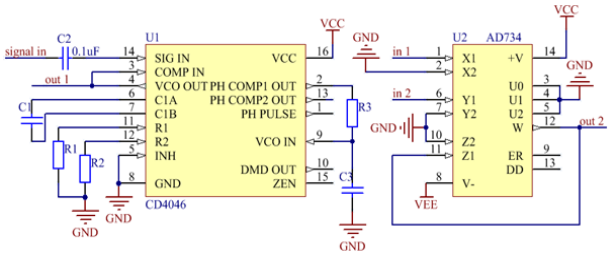

Figure 5. The circuit of PLL and multiplier.

In this design, R_3 and C_3 are used as consisting of low pass filter. The value of R_3 and C_3 are determined by the time constant of low pass filter. After the frequency capturing range of PLL is acquired, the value of R_1, R_2 and C_1 can be roughly calculated by the formula (18) and (19). Finally, the selected accurate value can be amended by experiment.

$$f_{\min} = \frac{1}{R_2(C_1 + 32pF)} \tag{18}$$

$$f_{\max} = \frac{1}{R_1(C_1 + 32pF)} + f_{\min} \tag{19}$$

In our testing platform, which consists of signal generator, oscilloscope and other devices, through the strictly experiment the selected value of R_1, R_2 and C_1 are achieved:

$$R_1 = 4.7\text{k}\Omega$$
$$R_2 = 82k\Omega$$
$$C_1 = 4400pF$$

Then:

$$f_{\min} = 2.75\text{k}Hz$$
$$f_{\max} = 50.0757kHz$$

4 Experimental results and analysis

Fig. 6 shows the experimental results of PLL circuit. Signal 1 is the input. Signal 2 is the output of the PLL circuit. The input signal is generated by the sinusoidal signal generator. The output of PLL is square wave, and the value is only related to the power supply voltage. It can be seen that the phase difference between the input and output is almost zero. The frequency of the output equals to the input. And the output of low pass filter is only related to the amplitude of the modulated signal. From the calculation above, it can be known that the frequency range is 2.75 kHz~50.0757 kHz. Through the experiment, it is found that the circuit can track the signal of 10 kHz~40 kHz very well.

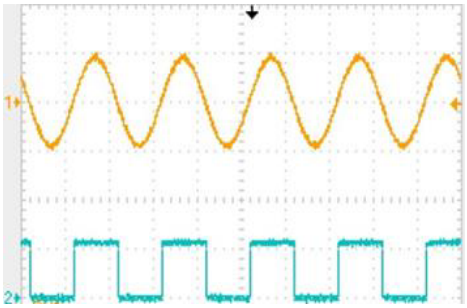

Figure 6. The experimental results of PLL circuit.

Multiplier AD734 is used in this design. It provides the transfer function $W=XY/U$. The circuit diagram of multiplier is shown in Figure 5. Figure 7 shows the experimental results of multiplier. Figure 8 is the output of low pass filter MAX297.

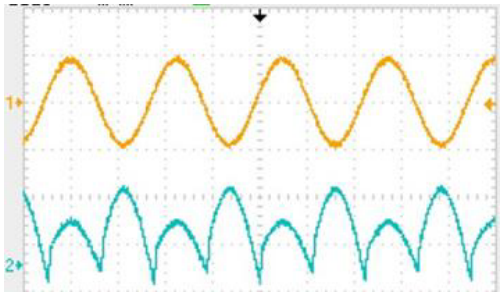

Figure 7. The experimental results of multiplier.

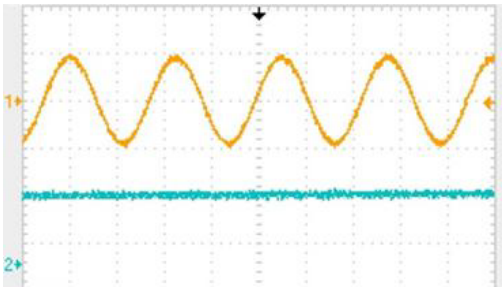

Figure 8. The output of low pass filter MAX297.

From the above experimental results, it can be seen that the applied PLL technology to the phase sensitive demodulation circuit makes the measurement circuit has high accuracy of measurement and stable phase tracking characteristics.

5 Conclusion

As long as the resistors, capacitors exist in the modulation and demodulation circuit, phase shift on the signal will no doubt occurs. And it cannot be eliminated quantitatively because the size of the phase shift is difficult to be measured in general circuit. In the phase-locked-loop circuit, the function of tracking frequency and locking phase are achieved through the feedback loop. After phase-locked-loop added in the phase sensitive detection circuit, the carrier signal is no longer used as reference signal for demodulation, but the output of the PLL circuit. Thus, the frequency and phase of two input signals of the multiplier can be same, and the output of the multiplier is only associated with the amplitude of the input signals. After such modification, the sensitivity of the system enhanced. It also makes the measurement results more accurate. Through the experiment, it is obvious that this method has strong practicability in the precision measurement of capacitance micrometer.

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